ST7567S

132X65 Dot Matrix LCD Controller/Driver

Datasheet

Version 1.4

2016/07

Sitronix Technology Corporation

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1 INTRODUCTION

ST7567S is a single-chip dot matrix LCD driver which incorporates LCD controller and common/segment drivers. ST7567S can be connected directly to a microprocessor with 8-bit parallel interface, 4-line serial interface (SPI-4), 3-line serial interface (SPI-3) or I2C serial interface. Display data sent from MPU is stored in the internal Display Data RAM (DDRAM) of 132x65 bits. The display data bits which are stored in DDRAM are directly related to the pixels of LCD panel. ST7567S contains 132 segment-outputs, 64 common-outputs and 1 icon-common-output. With built-in oscillation circuit and low power consumption power circuit, ST7567S generates LCD driving signal without external clock or power, so that it is possible to make a display system with the fewest components and minimal power consumption.

2 FEATURES

Single-chip LCD Controller & Driver

On-chip Display Data RAM (DDRAM)

- Capacity: 132x65=8580 bits
- Directly display RAM pattern from DDRAM

Selectable Display Duty (by SEL2 & SEL1)

- 1/65 duty : 132 segment x 65 common
- 1/55 duty : 132 segment x 55 common
- 1/49 duty : 132 segment x 49 common
- 1/33 duty : 132 segment x 33 common

Microprocessor Interface

- Bidirectional 8-bit parallel interface supports: 8080-series and 6800-series MPU
- 4-line SPI (SPI-4)
- 3-line SPI (SPI-3)
- I2C

Abundant Functions

- Display ON/OFF, Normal/Reverse Display Mode, Set Display Start Line, Read IC Status, Set all Display Points ON, Set LCD Bias, Electronic Volume Control, Read-modify-Write, Select Segment Driver Direction, Power Saving Mode, Select Common Driver Direction, Select Voltage Regulator Resistor Ratio (for V0).

External Hardware Reset Pin (RSTB)

Built-in Oscillation Circuit

- No external component required

Low Power Consumption Analog Circuit

- Voltage Booster (4X, 5X)
- High-accuracy Voltage Regulator for LCD Vop: (Thermal Gradient: -0.05%/℃)
- Voltage Follower for LCD Bias Voltage

Wide Operation Voltage Range

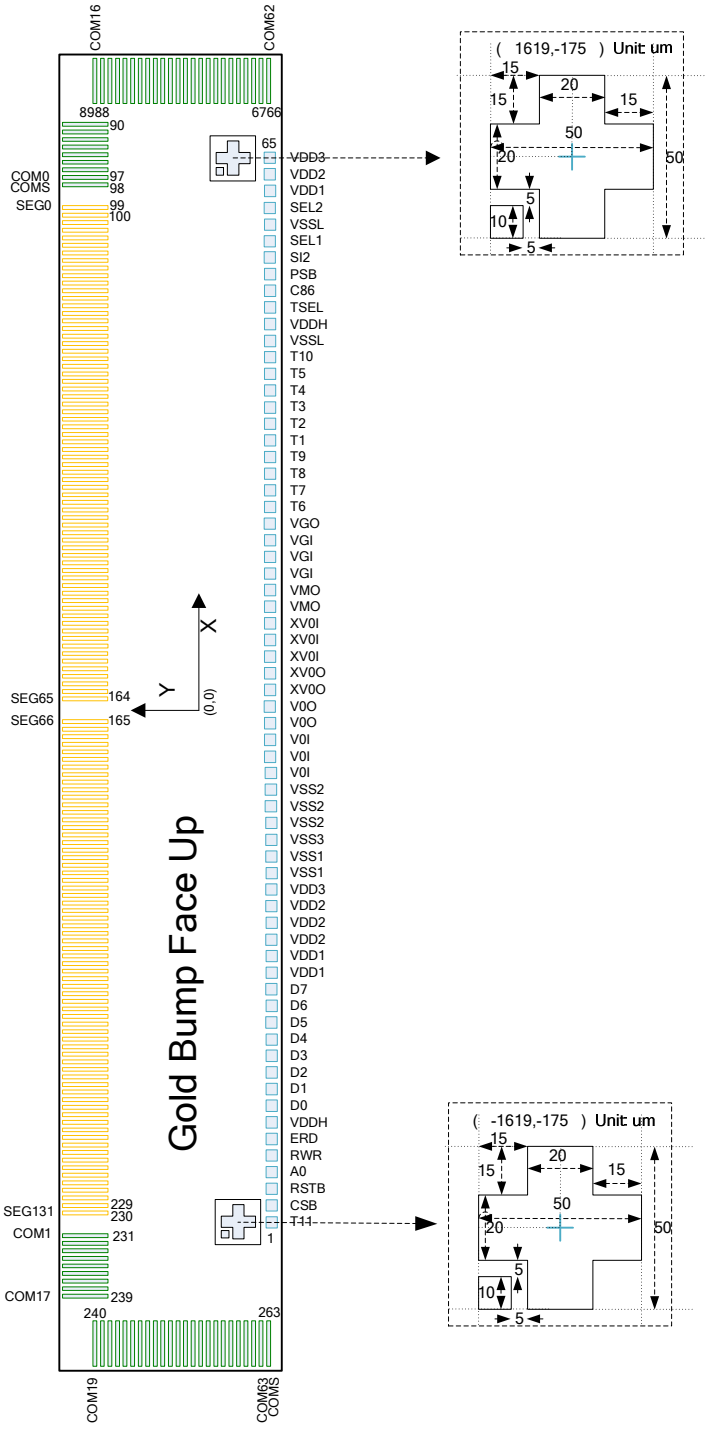
- VDD1-VSS1=1.8V~3.3V (TYP.)
- VDD2-VSS2=2.4V~3.3V (TYP.)
- VDD3-VSS3=2.4V~3.3V (TYP.)

Temperature Range: -30~85℃

Package Type: COG

3 COG OUTLINE

3-1 PAD ARRANGEMENT



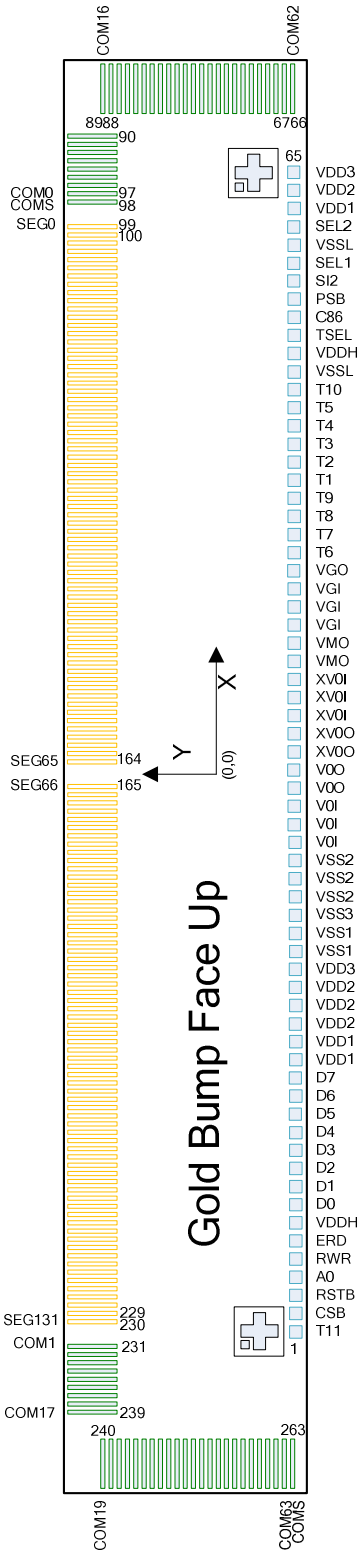
Part Number	
ST7567S-G4	
Chip Size	3800 x 640 ± 40
Chip Thickness	300
Bump Height	12
Bump Size	
PAD No.	**Size**
66~89,90~98,231~239, 240~263	12x110
99~164,165~230,	11 x110
1~6,8~43,	40 x 45
44~52	25 x 45
7,53~65	30 x 45
Bump Space	
PAD No.	**Length**
66~89,90~98,231~239, 240~263	11
99~164,165~230,	11

***** Unit: um

*** Refer to section "PAD CENTER COORDINATES" for ITO layout.**

Figure 1 Chip Outline

3-2 PAD CENTER COORDINATES



PAD NO.	PIN Name	X	Y
1	T11	-1618.20	-259.50
2	CSB	-1563.20	-259.50
3	RSTB	-1508.20	-259.50
4	A0	-1453.20	-259.50
5	RWR	-1398.20	-259.50
6	ERD	-1343.20	-259.50
7	VDDH	-1293.20	-259.50
8	D0	-1243.20	-259.50
9	D1	-1188.20	-259.50
10	D2	-1133.20	-259.50
11	D3	-1078.20	-259.50
12	D4	-1023.20	-259.50
13	D5	-968.20	-259.50
14	D6	-913.20	-259.50
15	D7	-858.20	-259.50
16	VDD1	-803.20	-259.50
17	VDD1	-748.20	-259.50
18	VDD2	-693.20	-259.50
19	VDD2	-638.20	-259.50
20	VDD2	-583.20	-259.50
21	VDD3	-528.20	-259.50
22	VSS1	-473.20	-259.50
23	VSS1	-418.20	-259.50
24	VSS3	-363.20	-259.50
25	VSS2	-308.20	-259.50
26	VSS2	-253.20	-259.50
27	VSS2	-198.20	-259.50
28	V0I	-143.20	-259.50
29	V0I	-88.20	-259.50
30	V0I	-33.20	-259.50
31	V0O	21.80	-259.50
32	V0O	76.80	-259.50
33	XV0O	131.80	-259.50
34	XV0O	186.80	-259.50
35	XV0I	241.80	-259.50
36	XV0I	296.80	-259.50
37	XV0I	351.80	-259.50
38	VMO	406.80	-259.50
39	VMO	461.80	-259.50
40	VGI	516.80	-259.50

Figure 2 PAD Location

PAD NO.	PIN Name	X	Y
41	VGI	571.80	-259.50
42	VGI	626.80	-259.50
43	VGO	681.80	-259.50
44	T6	729.30	-259.50
45	T7	769.30	-259.50
46	T8	809.30	-259.50
47	T9	849.30	-259.50
48	T1	889.30	-259.50
49	T2	929.30	-259.50
50	T3	969.30	-259.50
51	T4	1009.30	-259.50
52	T5	1049.30	-259.50
53	T10	1091.80	-259.50
54	VSSL	1136.80	-259.50
55	VDDH	1181.80	-259.50
56	TSEL	1226.80	-259.50
57	C86	1271.80	-259.50
58	PSB	1316.80	-259.50
59	SI2	1361.80	-259.50
60	SEL1	1406.80	-259.50
61	VSSL	1451.80	-259.50
62	SEL2	1496.80	-259.50
63	VDD1	1541.80	-259.50
64	VDD2	1586.80	-259.50
65	VDD3	1631.80	-259.50
66	COM62	1767.00	-264.50
67	COM60	1767.00	-241.50
68	COM58	1767.00	-218.50
69	COM56	1767.00	-195.50
70	COM54	1767.00	-172.50
71	COM52	1767.00	-149.50
72	COM50	1767.00	-126.50
73	COM48	1767.00	-103.50
74	COM46	1767.00	-80.50
75	COM44	1767.00	-57.50
76	COM42	1767.00	-34.50
77	COM40	1767.00	-11.50
78	COM38	1767.00	11.50
79	COM36	1767.00	34.50
80	COM34	1767.00	57.50

PAD NO.	PIN Name	X	Y
81	COM32	1767.00	80.50
82	COM30	1767.00	103.50
83	COM28	1767.00	126.50
84	COM26	1767.00	149.50
85	COM24	1767.00	172.50
86	COM22	1767.00	195.50
87	COM20	1767.00	218.50
88	COM18	1767.00	241.50
89	COM16	1767.00	264.50
90	COM14	1678.95	187.00
91	COM12	1655.95	187.00
92	COM10	1632.95	187.00
93	COM8	1609.95	187.00
94	COM6	1586.95	187.00
95	COM4	1563.95	187.00
96	COM2	1540.95	187.00
97	COM0	1517.95	187.00
98	COMS	1494.95	187.00
99	SEG0	1450.75	187.00
100	SEG1	1428.75	187.00
101	SEG2	1406.75	187.00
102	SEG3	1384.75	187.00
103	SEG4	1362.75	187.00
104	SEG5	1340.75	187.00
105	SEG6	1318.75	187.00
106	SEG7	1296.75	187.00
107	SEG8	1274.75	187.00
108	SEG9	1252.75	187.00
109	SEG10	1230.75	187.00
110	SEG11	1208.75	187.00
111	SEG12	1186.75	187.00
112	SEG13	1164.75	187.00
113	SEG14	1142.75	187.00
114	SEG15	1120.75	187.00
115	SEG16	1098.75	187.00
116	SEG17	1076.75	187.00
117	SEG18	1054.75	187.00
118	SEG19	1032.75	187.00
119	SEG20	1010.75	187.00
120	SEG21	988.75	187.00

PAD NO.	PIN Name	X	Y
121	SEG22	966.75	187.00
122	SEG23	944.75	187.00
123	SEG24	922.75	187.00
124	SEG25	900.75	187.00
125	SEG26	878.75	187.00
126	SEG27	856.75	187.00
127	SEG28	834.75	187.00
128	SEG29	812.75	187.00
129	SEG30	790.75	187.00
130	SEG31	768.75	187.00
131	SEG32	746.75	187.00
132	SEG33	724.75	187.00
133	SEG34	702.75	187.00
134	SEG35	680.75	187.00
135	SEG36	658.75	187.00
136	SEG37	636.75	187.00
137	SEG38	614.75	187.00
138	SEG39	592.75	187.00
139	SEG40	570.75	187.00
140	SEG41	548.75	187.00
141	SEG42	526.75	187.00
142	SEG43	504.75	187.00
143	SEG44	482.75	187.00
144	SEG45	460.75	187.00
145	SEG46	438.75	187.00
146	SEG47	416.75	187.00
147	SEG48	394.75	187.00
148	SEG49	372.75	187.00
149	SEG50	350.75	187.00
150	SEG51	328.75	187.00
151	SEG52	306.75	187.00
152	SEG53	284.75	187.00
153	SEG54	262.75	187.00
154	SEG55	240.75	187.00
155	SEG56	218.75	187.00
156	SEG57	196.75	187.00
157	SEG58	174.75	187.00
158	SEG59	152.75	187.00
159	SEG60	130.75	187.00
160	SEG61	108.75	187.00

PAD NO.	PIN Name	X	Y
161	SEG62	86.75	187.00
162	SEG63	64.75	187.00
163	SEG64	42.75	187.00
164	SEG65	20.75	187.00
165	SEG66	-20.75	187.00
166	SEG67	-42.75	187.00
167	SEG68	-64.75	187.00
168	SEG69	-86.75	187.00
169	SEG70	-108.75	187.00
170	SEG71	-130.75	187.00
171	SEG72	-152.75	187.00
172	SEG73	-174.75	187.00
173	SEG74	-196.75	187.00
174	SEG75	-218.75	187.00
175	SEG76	-240.75	187.00
176	SEG77	-262.75	187.00
177	SEG78	-284.75	187.00
178	SEG79	-306.75	187.00
179	SEG80	-328.75	187.00
180	SEG81	-350.75	187.00
181	SEG82	-372.75	187.00
182	SEG83	-394.75	187.00
183	SEG84	-416.75	187.00
184	SEG85	-438.75	187.00
185	SEG86	-460.75	187.00
186	SEG87	-482.75	187.00
187	SEG88	-504.75	187.00
188	SEG89	-526.75	187.00
189	SEG90	-548.75	187.00
190	SEG91	-570.75	187.00
191	SEG92	-592.75	187.00
192	SEG93	-614.75	187.00
193	SEG94	-636.75	187.00
194	SEG95	-658.75	187.00
195	SEG96	-680.75	187.00
196	SEG97	-702.75	187.00
197	SEG98	-724.75	187.00
198	SEG99	-746.75	187.00
199	SEG100	-768.75	187.00
200	SEG101	-790.75	187.00

PAD NO.	PIN Name	X	Y
201	SEG102	-812.75	187.00
202	SEG103	-834.75	187.00
203	SEG104	-856.75	187.00
204	SEG105	-878.75	187.00
205	SEG106	-900.75	187.00
206	SEG107	-922.75	187.00
207	SEG108	-944.75	187.00
208	SEG109	-966.75	187.00
209	SEG110	-988.75	187.00
210	SEG111	-1010.75	187.00
211	SEG112	-1032.75	187.00
212	SEG113	-1054.75	187.00
213	SEG114	-1076.75	187.00
214	SEG115	-1098.75	187.00
215	SEG116	-1120.75	187.00
216	SEG117	-1142.75	187.00
217	SEG118	-1164.75	187.00
218	SEG119	-1186.75	187.00
219	SEG120	-1208.75	187.00
220	SEG121	-1230.75	187.00
221	SEG122	-1252.75	187.00
222	SEG123	-1274.75	187.00
223	SEG124	-1296.75	187.00
224	SEG125	-1318.75	187.00
225	SEG126	-1340.75	187.00
226	SEG127	-1362.75	187.00
227	SEG128	-1384.75	187.00
228	SEG129	-1406.75	187.00
229	SEG130	-1428.75	187.00
230	SEG131	-1450.75	187.00
231	COM1	-1494.95	187.00
232	COM3	-1517.95	187.00
233	COM5	-1540.95	187.00
234	COM7	-1563.95	187.00
235	COM9	-1586.95	187.00
236	COM11	-1609.95	187.00
237	COM13	-1632.95	187.00
238	COM15	-1655.95	187.00
239	COM17	-1678.95	187.00
240	COM19	-1767.00	264.50

PAD NO.	PIN Name	X	Y
241	COM21	-1767.00	241.50
242	COM23	-1767.00	218.50
243	COM25	-1767.00	195.50
244	COM27	-1767.00	172.50
245	COM29	-1767.00	149.50
246	COM31	-1767.00	126.50
247	COM33	-1767.00	103.50
248	COM35	-1767.00	80.50
249	COM37	-1767.00	57.50
250	COM39	-1767.00	34.50
251	COM41	-1767.00	11.50
252	COM43	-1767.00	-11.50
253	COM45	-1767.00	-34.50
254	COM47	-1767.00	-57.50
255	COM49	-1767.00	-80.50
256	COM51	-1767.00	-103.50
257	COM53	-1767.00	-126.50
258	COM55	-1767.00	-149.50
259	COM57	-1767.00	-172.50
260	COM59	-1767.00	-195.50
261	COM61	-1767.00	-218.50
262	COM63	-1767.00	-241.50
263	COMS	-1767.00	-264.50

Note:

1. Unit: um
2. This is the default PAD Center Coordinate Table with 1/65 Duty. Other duty output mapping can be found in Section 6 FUNCTION DESCRIPTION.
3. Tolerance: +/- 0.05 um.
4. **The definition of pin name is in full duty (65 duty).**
5. **The definition of output pin in different duty (55 Duty, 49 Duty and 33 Duty) please refers Figure 15~17**.

4 BLOCK DIAGRAM

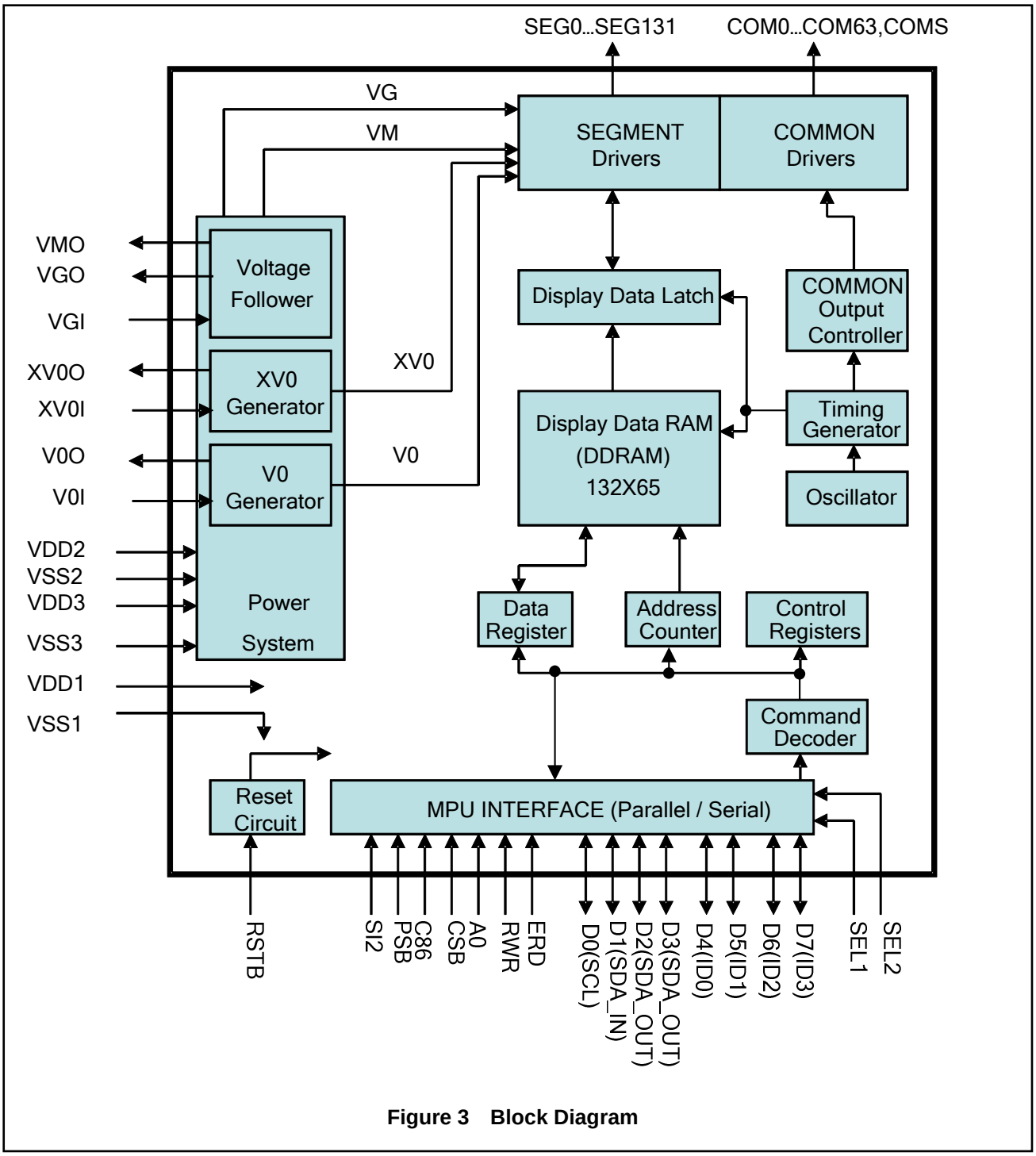


Figure 3 Block Diagram

5 HARDWARE PIN DESCRIPTION

5-1 LCD Driver Output Pins

<table>
<tr><th>Pin Name</th><th>Type</th><th>Description</th><th>Pins</th></tr>
<tr><td>SEG0 to
SEG131</td><td>O</td><td>LCD segment driver outputs.
The display data and the frame control the output voltage.
<table>
<tr><th rowspan="2">Display data</th><th rowspan="2">Frame</th><th colspan="2">Segment Driver Output Voltage</th></tr>
<tr><th>Normal Display</th><th>Inverse Display</th></tr>
<tr><td>H</td><td>+</td><td>VG</td><td>VSS</td></tr>
<tr><td>H</td><td>-</td><td>VSS</td><td>VG</td></tr>
<tr><td>L</td><td>+</td><td>VSS</td><td>VG</td></tr>
<tr><td>L</td><td>-</td><td>VG</td><td>VSS</td></tr>
<tr><td colspan="2">Display OFF,
Power Save</td><td>VSS</td><td>VSS</td></tr>
</table></td><td>132</td></tr>
<tr><td>COM0 to
COM63</td><td>O</td><td>LCD common driver outputs.
The internal scanning signal and the frame control the output voltage.
<table>
<tr><th rowspan="2">Scan signal</th><th rowspan="2">Frame</th><th colspan="2">Common Driver Output Voltage</th></tr>
<tr><th>Normal Display</th><th>Inverse Display</th></tr>
<tr><td>H</td><td>+</td><td colspan="2">XV0</td></tr>
<tr><td>H</td><td>-</td><td colspan="2">V0</td></tr>
<tr><td>L</td><td>+</td><td colspan="2">VM</td></tr>
<tr><td>L</td><td>-</td><td colspan="2">VM</td></tr>
<tr><td colspan="2">Display OFF,
Power Save</td><td colspan="2">VSS</td></tr>
</table></td><td>64</td></tr>
<tr><td>COMS</td><td>O</td><td>LCD common driver outputs for icons.
The output signals of these two pins are the same.
When icon feature is not used, these pins should be left open.</td><td>2</td></tr>
</table>

5-2 Microprocessor Interface Pins

Pin Name	Type	Description	Pins
RSTB	**I**	Hardware reset input pin. When RSTB is “L”, internal initialization is executed and the internal registers will be initialized.	**1**
CSB	**I**	Chip select input pin. Interface access is enabled when CSB is “L”. When CSB is non-active (CSB=“H”), D[7:0] pins are high impedance.	**1**
A0	**I**	It determines whether the access is related to data or command. A0=“H” : Indicates that signals on D[7:0] are display data. A0=“L” : Indicates that signals on D[7:0] are command.	**1**

<table>
<tr><th>Pin Name</th><th>Type</th><th>Description</th><th>Pins</th></tr>
<tr><td>RWR</td><td>I</td><td>Read/Write execution control pin. When PSB is “H”,
<table>
<tr><th>C86</th><th>MPU Type</th><th>RWR</th><th>Description</th></tr>
<tr><td>H</td><td>6800 series</td><td>R/W</td><td>Read/Write control input pin.
R/W=“H”: read.
R/W=“L”: write.</td></tr>
<tr><td>L</td><td>8080 series</td><td>/WR</td><td>Write enable input pin.
Signals on D[7:0] will be latched at the rising edge of /WR signal.</td></tr>
</table>
RWR is used to decide slave address (SA1) in I2C serial interface.
RWR is not used in 3-line and 4-line SPI interface and should fix to “H” by VDD1 or VDDH.</td><td>1</td></tr>
<tr><td>ERD</td><td>I</td><td>Read/Write execution control pin. When PSB is “H”,
<table>
<tr><th>C86</th><th>MPU Type</th><th>ERD</th><th>Description</th></tr>
<tr><td>H</td><td>6800 series</td><td>E</td><td>Read/Write control input pin.
R/W=”H“: When E is “H”, D[7:0] are in output mode.
R/W=”L“: Signals on D[7:0] are latched at the falling edge of E signal.</td></tr>
<tr><td>L</td><td>8080 series</td><td>/RD</td><td>Read enable input pin.
When /RD is “L”, D[7:0] are in output mode.</td></tr>
</table>
ERD is used to decide slave address (SA0) in I2C serial interface.
ERD is not used in 3-Line and 4-Line SPI interface and should fix to “H” by VDD1 or VDDH.</td><td>1</td></tr>
<tr><td rowspan="2">D[7:0]</td><td>I/O</td><td>When using 8-bit parallel interface: (6800 or 8080 mode)
8-bit bi-directional data bus. Connect to the data bus of 8-bit microprocessor.
When CSB is non-active (CSB=“H”), D[7:0] pins are high impedance.</td><td rowspan="2">8</td></tr>
<tr><td>I/O</td><td>When using serial interface: 4-line SPI, 3-line SPI or I2C serial interface
D[0]=SCL: Serial clock input.
D[1]=SDA_IN: Serial data input.
D[2:3]=SDA_OUT: Serial data output.
D[1:3] must be connected together as SDA.
D[4:7]=(1,1,1,1): ID Pin. D[4:7] should fix to “H” or “L” by VDDH or VSSL.
ID[0:3] can be read 4-bit ID only for serial interface from D[4:7].</td></tr>
</table>

Note:

1. After VDD1 is turned ON, any MPU interface pins cannot be left floating.

5-3 Configuration Pins

<table>
<tr><th>Pin Name</th><th>Type</th><th>Description</th><th>Pins</th></tr>
<tr><td>VDDH</td><td>O</td><td>Logic “1” level for option pins which should connected to “H”.</td><td>2</td></tr>
<tr><td>VSSL</td><td>O</td><td>Logic “0” level for option pins which should connected to “L”.</td><td>2</td></tr>
<tr><td>PSB</td><td>I</td><td>PSB selects the interface type: Serial or Parallel.</td><td>1</td></tr>
<tr><td>C86</td><td>I</td><td>C86 selects the microprocessor type in parallel interface mode.</td><td>1</td></tr>
<tr><td>SI2</td><td>I</td><td>SI2 selects the interface type: I2C serial interface or not
<table>
<tr><th>SI2</th><th>PSB</th><th>C86</th><th>Selected Interface</th></tr>
<tr><td>“L”</td><td>“L”</td><td>“L”</td><td>Serial 3-Line SPI Interface</td></tr>
<tr><td>“L”</td><td>“L”</td><td>“H”</td><td>Serial 4-Line SPI Interface</td></tr>
<tr><td>“L”</td><td>“H”</td><td>“L”</td><td>Parallel 8080 Series MPU Interface</td></tr>
<tr><td>“L”</td><td>“H”</td><td>“H”</td><td>Parallel 6800 Series MPU Interface</td></tr>
<tr><td>“H”</td><td>“L”</td><td>“X”</td><td>I2C Serial Interface</td></tr>
</table>
Please refer to “APPLICATION NOTES” and “Microprocessor Interface” (Section 6) for detailed connection of the selected interface.</td><td>1</td></tr>
<tr><td>SEL[2:1]</td><td>I</td><td>These pins select the display duty and bias of ST7567S.
<table>
<tr><th>SEL2</th><th>SEL1</th><th>Duty</th><th>Bias</th></tr>
<tr><td>“L”</td><td>“L”</td><td>1/65</td><td>1/9 or 1/7</td></tr>
<tr><td>“L”</td><td>“H”</td><td>1/49</td><td>1/8 or 1/6</td></tr>
<tr><td>“H”</td><td>“L”</td><td>1/33</td><td>1/6 or 1/5</td></tr>
<tr><td>“H”</td><td>“H”</td><td>1/55</td><td>1/8 or 1/6</td></tr>
</table>
Note:
The detailed definition of output pin name can be found in Fig. 14~17.</td><td>2</td></tr>
</table>

5-4 Power System Pins

Pin Name	Type	Description	Pins
VDD1	**Power**	Digital power. If VDD1=VDD2, connect to VDD2 externally.	**3**
VDD2	**Power**	Analog power. If VDD1=VDD2, connect to VDD1 externally.	**4**
VDD3	**Power**	Power for reference voltage circuit.	**2**
VSS1	**Power**	Digital ground. Connect to VSS2 externally.	**2**
VSS2	**Power**	Analog ground. Connect to VSS1 externally.	**3**
VSS3	**Power**	Ground for reference voltage circuit.	**1**
V0O V0I	**Power**	V0 is the LCD driving voltage for common circuits at negative frame. V0O is the output of V0 regulator. V0I is the V0 input of common circuits. Be sure that: V0 ≥ VG >VM> VSS ≥ XV0 (under operation). V0O, V0I should be connected together in ITO layout.	**2** **3**
XV0O XV0I	**Power**	XV0 is the LCD driving voltage for common circuits at positive frame. XV0O is the output of XV0 regulator. XV0I is the XV0 input of common circuits. XV0O, XV0I should be connected together in ITO layout.	**2** **3**
VGO VGI	**Power**	VG is the LCD driving voltage for segment circuits. VGO is the output of VG regulator. VGI is the VG input of segment circuits. VGO, VGI should be connected together in ITO layout. 1.6V ≤ VG < VDD2-0.2V.	**1** **3**
VMO	**Power**	VM is the LCD driving voltage for common circuits. 0.8V ≤ VM < VG.	**2**

5-5 Test Pins

Pin Name	Type	Description	Pins
T1~T11	**T**	Do NOT use. Reserved for testing. Must be floating.	**11**
TSEL	**T**	TSEL must be connected to “L” by VSSL.	**1**

5-6 Recommend ITO Resistance

Pin Name	ITO Resistance
T[11:1],VMO	Floating
VDD1, VDD2, VDD3	< 100Ω
VSS1, VSS2, VSS3	< 70Ω
V0(V0I,V0O), XV0(XVI,XV0O), VG(VGI,VGO)	< 200 Ω
A0, RWR, ERD, CSB, D[7:0]	< 700Ω
PSB, C86, SEL[2:1],SI2,TSEL	< 5KΩ
D[0](I2C - SCL),D[3:1](I2C - SDA)	<100Ω
D[0](3-line or 4-line SPI - SCL),D[3:1](3-line or 4-line SPI - SDA)	<300Ω
RSTB *1	2~3KΩ

Note:

1. To prevent the ESD pulse resetting the internal register, applications should increase the resistance of RSTB signal (add a series resistor or increase ITO resistance). The value is different from modules.
2. The option setting to be “H” should connect to VDD1 or VDDH.
3. The option setting to be “L” should connect to VSS1 or VSSL.

6 FUNCTION DESCRIPTION

6-1Microprocessor Interface

6-1-1 Chip Select Input

CSB pin is used for chip selection. When CSB is “L”, the microprocessor interface is enabled and ST7567S can interface with an MPU. When CSB is “H”, the inputs of A0, ERD and RWR with any combination will be ignored and D[7:0] are high impedance. In the serial interface (3-Line, 4-Line SPI and I2C), the internal shift register and serial counter are reset when CSB is “H”.

6-1-2 Interface Selection

The interface selection is controlled by C86, PSB and SI2 pins. The selection for parallel or serial interface is shown in Table 1.

Table 1. Parallel/Serial Interface Mode

SI2	PSB	C86	CSB	A0	ERD	RWR	D[7:0]	MPU Interface
“L”	“L”	“L”	CSB	---	---	---	Refer to serial interface.	3-Line SPI interface
“L”	“L”	“H”		A0	---	---		4-Line SPI interface
“L”	“H”	“L”			/RD	/WR	D[7:0]	8080-series parallel interface
“L”	“H”	“H”			E	R/W		6800-series parallel interface
“H”	“L”	“X”	---	---	SA0	SA1	Refer to serial interface.	I2C serial interface

⇨ The un-used pins are marked as “---” and should be fixed to “H” by VDD1 or VDDH.

6-1-3 Parallel Interface

When PSB= “H”, the 8-bit bi-directional parallel interface is enabled and the type of MPU is selected by “C86” pin as shown in Table 2**.** The data transfer type is determined by signals on A0, ERD and RWR as shown in Table 3.

Table 2. Microprocessor Selection for Parallel Interface

PSB	C86	CSB	A0	ERD	RWR	D[7:0]	MPU Interface
“H”	“L”	CSB	A0	/RD	/WR	D[7:0]	8080-series parallel interface
“H”	“H”			E	R/W		6800-series parallel interface

Table 3. Parallel Data Transfer Type

Common Pins		6800-Series		8080-Series		Description
CSB	A0	E (ERD)	R/W (RWR)	/RD (ERD)	/WR (RWR)	
“L”	“H”	“H”	“H”	“L”	“H”	Display data read out
	“H”	“H”	“L”	“H”	“L”	Display data write
	“L”	“H”	“H”	“L”	“H”	Internal status read
	“L”	“H”	“L”	“H”	“L”	Writes to internal register (instruction)

6-1-4 Setting Serial Interface

Serial Mode	SI2	PSB	C86	CSB	A0	ERD	RWR	D[7:0]
3-Line SPI interface	“L”	“L”	“L”	CSB	---	---	---	ID3,ID2,ID1,ID0,SDA,SDA,SDA,SCL
4-Line SPI interface	“L”	“L”	“H”	CSB	A0	---	---	ID3,ID2,ID1,ID0,SDA,SDA,SDA,SCL
I2C serial interface	“H”	“L”	“X”	---	---	SA0	SA1	ID3,ID2,ID1,ID0,SDA,SDA,SDA,SCL

* The un-used pins are marked as “---” and should be fixed to “H” by VDD1 or VDDH.
* C86 is marked as “X” and can be fixed to “H” or “L”.

Note:
1. The option setting to be “H” should connect to VDD1 or VDDH.
2. The option setting to be “L” should connect to VSS1 or VSSL.

6-2 4-line SPI interface (SI2=“L”, PSB=“L” and C86=“H”)

When ST7567S is active (CSB=“L”), serial data (SDA) and serial clock (SCL) inputs are enabled. When ST7567S is not active (CSB=“H”), the internal 8-bit shift register and 3-bit counter are reset. Serial data on SDA is latched at the rising edge of serial clock on SCL. After the 8th serial clock, the serial data will be processed to be 8-bit parallel data. The address selection pin (A0), which is latched at the 8th clock, indicates the 8-bit parallel data is display data or instruction. The 8-bit parallel data will be display data when A0 is “H” and will be instruction when A0 is “L”. The read feature is not available in this mode. The DDRAM column address pointer will be increased by one automatically after each byte of DDRAM access. Please note that the SCL signal quality is very important and external noise maybe causes unexpected data/instruction latch.

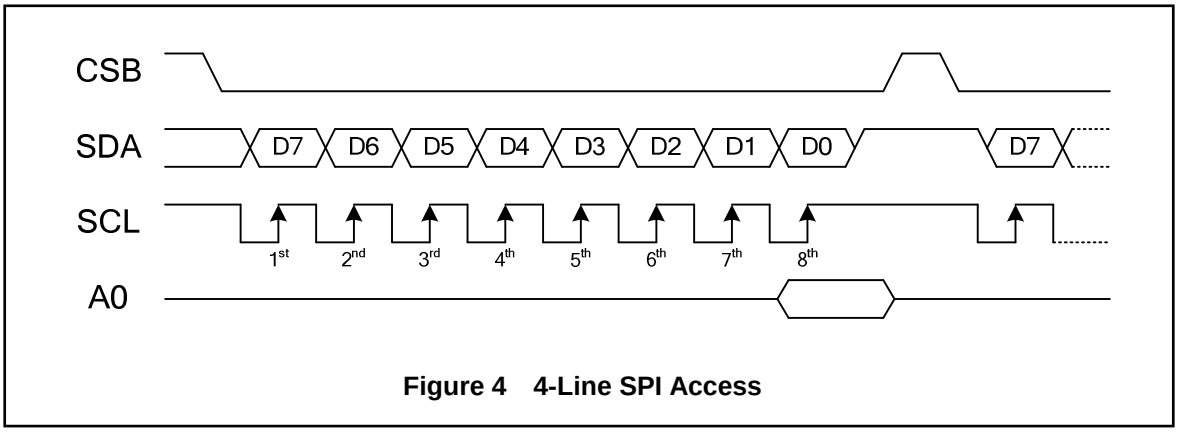


Figure 4 4-Line SPI Access

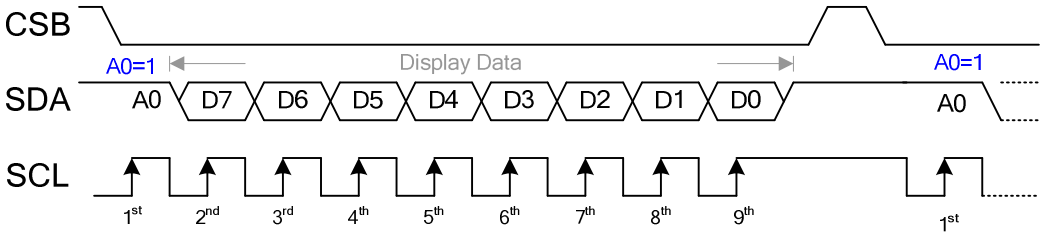
Note:
Some MPU will set the interface to be Hi-Z (high impedance) mode when power saving mode or after hardware reset. This is not allowed when the VDD1of ST7567S is turned ON. Because the floating input (especially for those control pins such as CSB, RSTB, RWR or ERD…) maybe cause abnormal latch and cause abnormal display.

6-3 3-line SPI interface (SI2="L", PSB="L" and C86="L")

The 3-Line SPI (9-bit) uses 3 pins (CSB, SDA & SCL) to communicate with MPU. When CSB is "L", IC is active and the SDA and SCL pins are enabled. Serial data is latched at the rising edge of serial clock. The internal shift register collects serial bits and reformat them into 8-bit data after the last (9th) clock. After CSB returns to "H", IC is inactive and the internal shift register and counter are reset. The parameter/command indicator is the "A0" bit at the 1st bit of each 9-bit serial data.

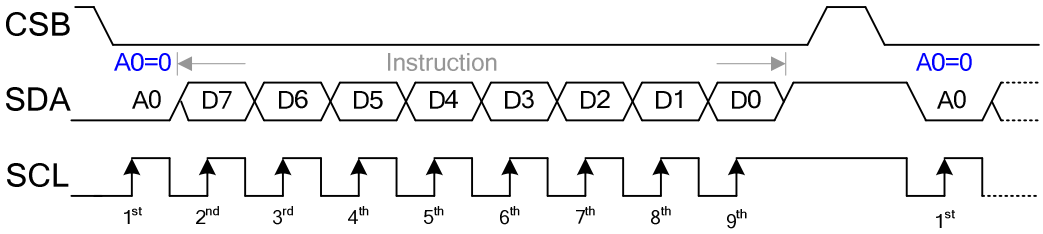
Write Parameter by 3-Line SPI (A0=1)

When A0 is "1", the transferred 8-bit is parameter.



Write Instruction by 3-Line SPI (A0=0)

When A0 is "0", the transferred 8-bit is instruction.



6-4 I2C serial interface (SI2="H, "PSB="L" and C86="X")

The I2C Interface is for bi-directional, two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock line (SCL). Both lines must be connected with a pull-up resistor which drives SDA and SCL to high when the bus is not busy. Data transfer can be initiated only when the bus is not busy.

6-4-1 Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse because changes of SDA line at this time will be interpreted as START or STOP. Bit transfer is illustrated in Fig 5.

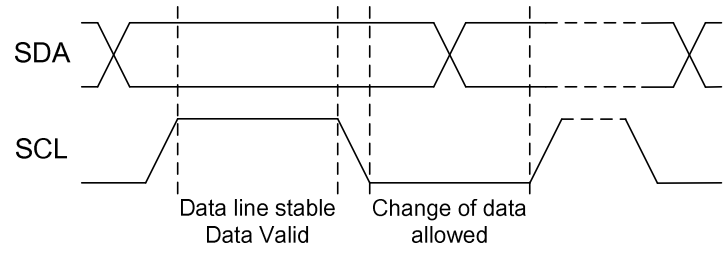


Figure 5 Bit Transfer

6-4-2 Start and Stop Conditions

Both SDA and SCL lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of SDA, while SCL is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of SDA while SCL is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated in Fig 6.

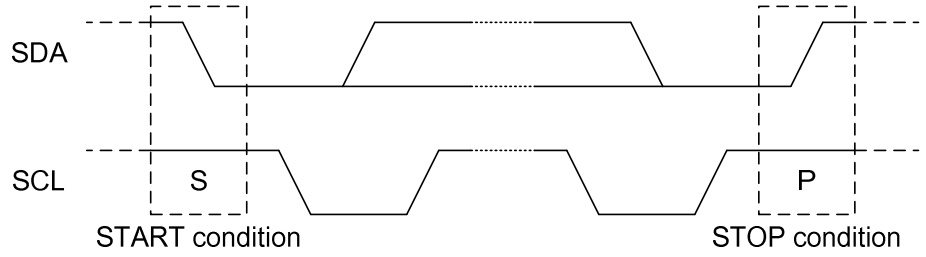


Figure 6 Definition of STRAT and STOP Condition

6-4-3 System Configuration

The system configuration is illustrated in Fig. 7 and some word-definitions are explained below:

- Transmitter: the device which sends the data to the bus.
- Receiver: the device which receives the data from the bus.
- Master: the device which initiates a transfer generates clock signals and terminates a transfer.
- Slave: the device which is addressed by a master.
- Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message.
- Arbitration: the procedure to ensure that, if more than one master tries to control the bus simultaneously, only one is allowed to do so and the message is not corrupted.
- Synchronization: procedure to synchronize the clock signals of two or more devices.

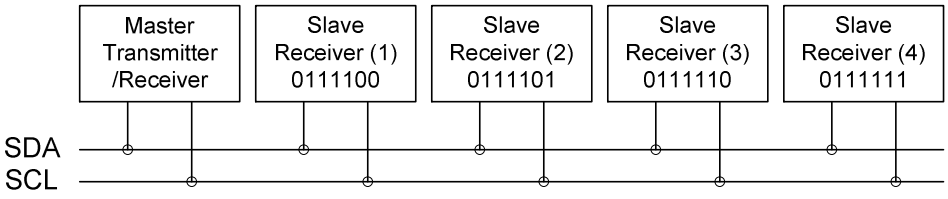


Figure 7 System Configuration

6-4-4 Acknowledgement

Each byte of eight bits is followed by an acknowledge-bit. The acknowledge-bit is a HIGH signal put on SDA by the transmitter during the time when the master generates an extra acknowledge-related clock pulse. A slave receiver which is addressed must generate an acknowledge-bit after the reception of each byte. The device that acknowledges must pull-down the SDA line during the acknowledge-clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse (set-up and hold times must be taken into consideration). Acknowledgement on the I2C Interface is illustrated in Fig 8.

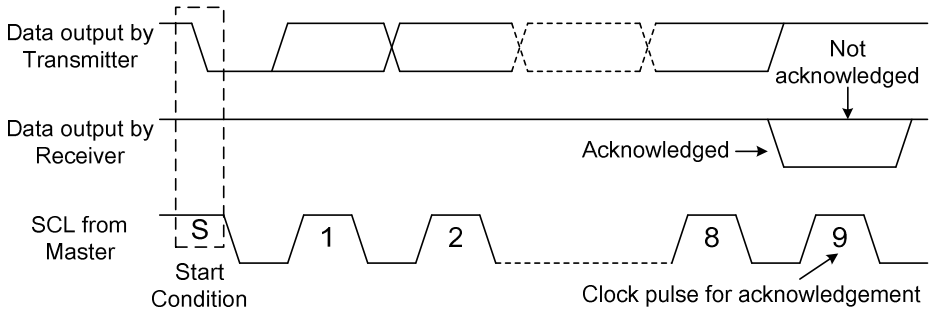


Figure 8 Acknowledgement of I2C Interface

6-4-5 I2C Interface Protocol

ST7567S supports command/data write to addressed slaves on the bus.

Before any data is transmitted on the I2C Interface, the device, which should respond, is addressed first. Four 7-bit slave addresses (0111**100**, 0111**101**, 0111**110** and 0111**111**) are reserved for ST7567S. The least significant 2 bits of the slave address is set by connecting SA0 and SA1 to either logic 0 (VSSL) or logic 1 (VDDH). The I2C Interface protocol is illustrated in Fig 9.

The sequence is initiated with a START condition (S) from the I2C Interface master, which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I2C Interface transfer. After acknowledgement, one or more command words are followed and define the status of the addressed slaves. A command word consists of a control byte, which defines Co and A0, and a data byte.

The last control byte is tagged with a cleared most significant bit (i.e. the continuation bit Co). After a control byte with a cleared Co bit, only data byte(s) will follow. The state of the A0 bit defines whether the following data bytes are interpreted as commands or as RAM data. All addressed slaves on the bus also acknowledge the control and data bytes. After the last control byte either a series of display data bytes or command data bytes may follow (depending on the A0 bit setting).

If the A0 bit of the last control byte is set to logic 1, these data bytes (display data bytes) will be stored in the display RAM at the address specified by the internal data pointer. The data pointer is automatically updated and the data is directed to the intended ST7567S device.

If the A0 bit of the last control byte is set to logic 0, these data bytes (command data byte) will be decoded and the setting of ST7567S will be changed according to the received commands.

Only the addressed slave makes the acknowledgement after each byte. At the end of the transmission the bus master issues a STOP condition (P). If no acknowledge is generated by the master after a byte, the driver stops transferring data to the master.

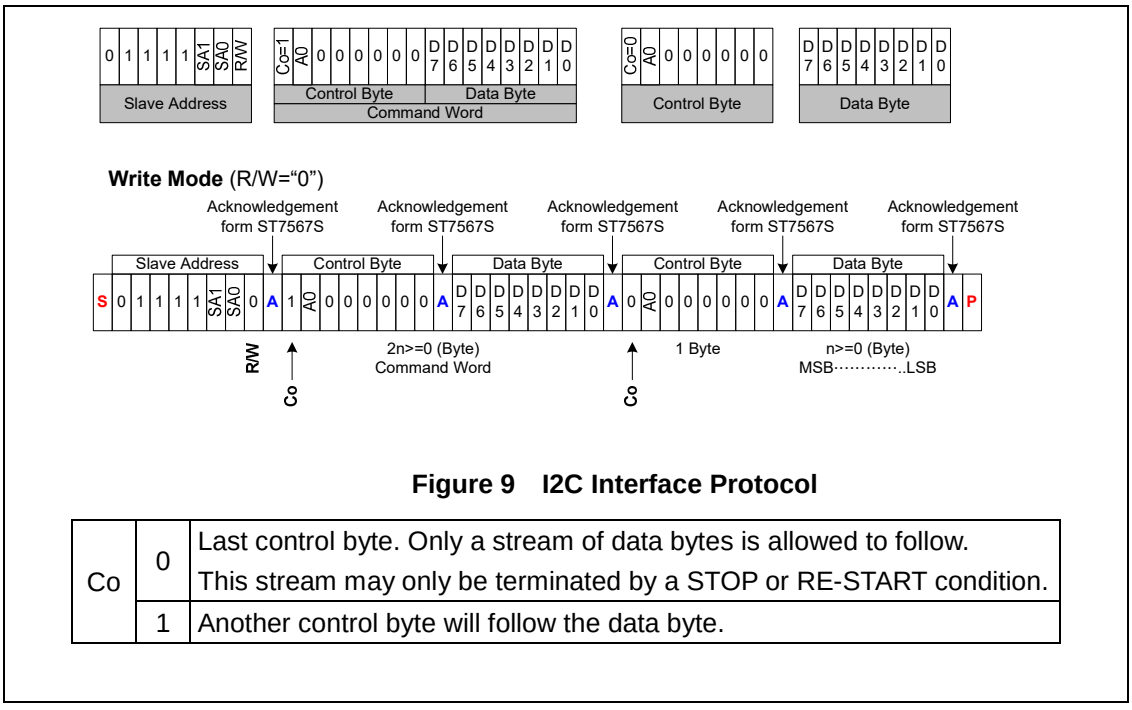


Figure 9 I2C Interface Protocol

Co	0	Last control byte. Only a stream of data bytes is allowed to follow. This stream may only be terminated by a STOP or RE-START condition.
	1	Another control byte will follow the data byte.

6-5 Data Transfer

ST7567S uses bus latch and internal data bus for parallel interface data transfer. When writing data from MPU to the DDRAM, data is automatically transferred from the bus latch to the DDRAM as shown in Fig.10. When reading data from the on-chip DDRAM to MPU, the first read cycle reads the content in bus latch (dummy read) and the data that MPU should read will be output at the next read cycle as shown in Fig. 11. That means: after setting the target address, a dummy read cycle is required before the following read-operation. Therefore, the data of the specified address cannot be read at the first read of display data right after setting the address, but can be read at the second read of display data.

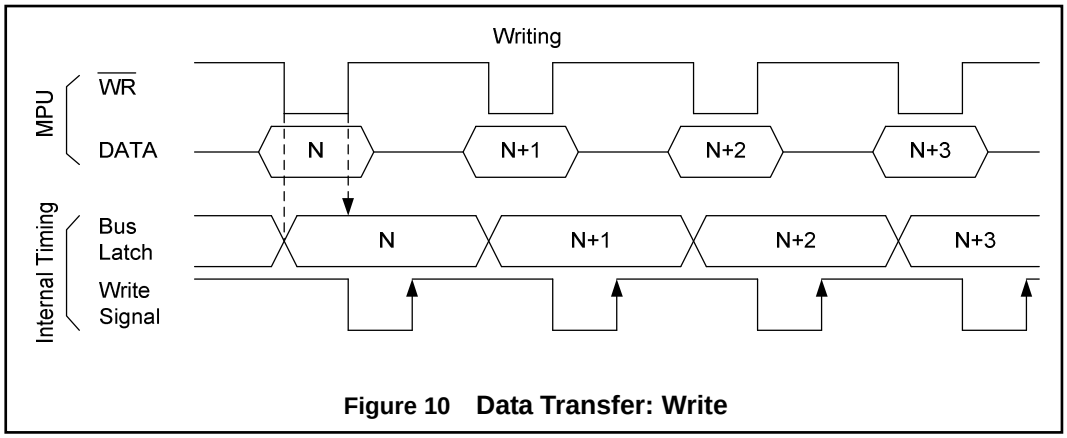


Figure 10 Data Transfer: Write

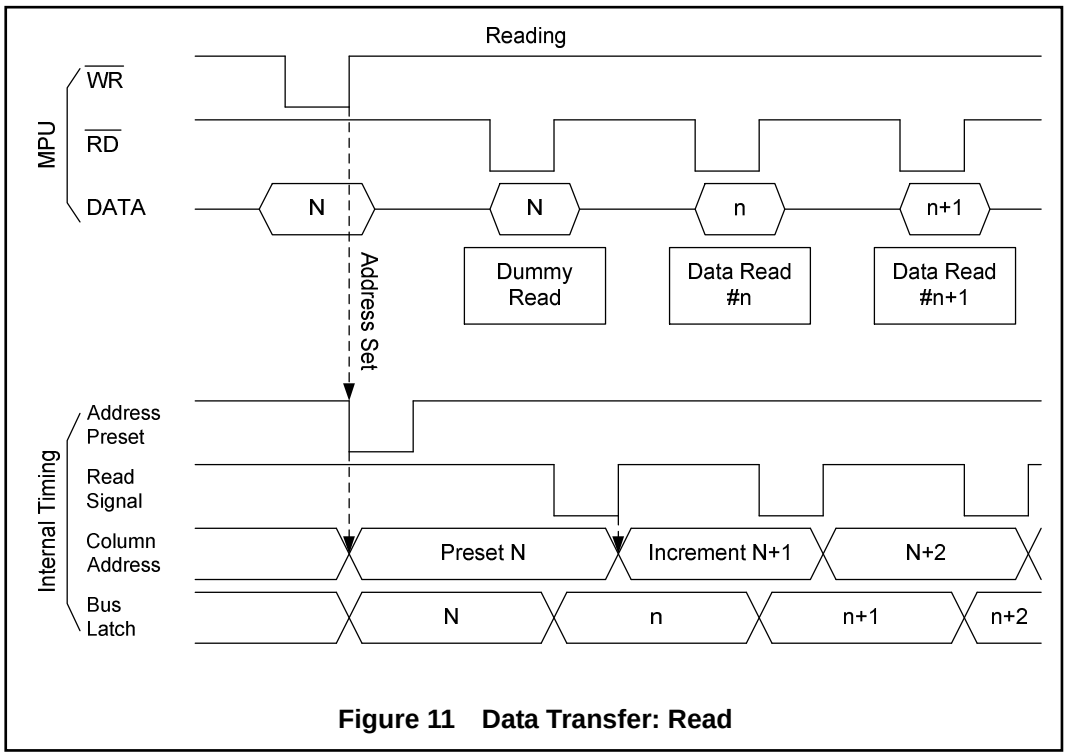


Figure 11 Data Transfer: Read

Note: Dummy bit description (Read RAM Mode)

8080 interface: 8-bit

6800 interface: 8-bit

3-Line interface: 1-bit

4-Line interface: 1-bit

I2C interface: 8-bit

7 DISPLAY DATA RAM (DDRAM)

ST7567S is built-in a RAM with 132X65 bit capacity which stores the display data. The display data RAM (DDRAM) store the dot data of the LCD. It is an addressable array with 132 columns by 65 rows (8-page with 8-bit and 1-page with 1-bit). The X-address is directly related to the column output number. Each pixel can be selected when the page and column addresses are specified (please refer to Fig.12 detailed illustration). The rows are divided into: 8 pages (Page-0 ~ Page-7) each with 8 lines (for COM0~63) and Page-8 with only 1 line (COMS, for icon). The display data (D7~D0) corresponds to the LCD common-line direction and D0 is on top. All pages can be accessed through D[7:0] directly except icon page. Icon RAM uses only 1-bit of data bus (D0). Refer to Fig. 13 for detailed illustration. The microprocessor can write to and read from DDRAM by the I/O buffer. Since the LCD controller operates independently, data can be written into DDRAM at the same time as data is being displayed without causing the LCD flicker or data-conflict.

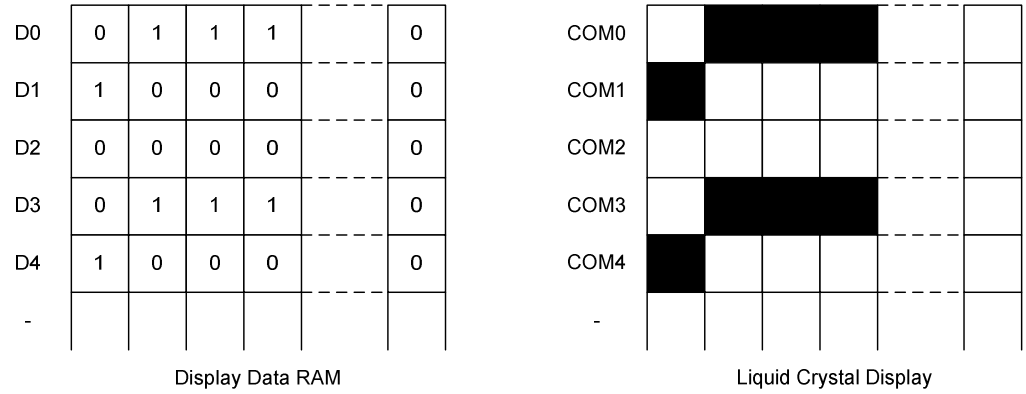


Figure 12 DDRAM Mapping (Default Setting)

Figure 13 DDRAM Format

7-1 Addressing

Data is downloaded into the Display Data RAM matrix in ST7567S as byte-format. The Display Data RAM has a matrix of 132 by 65 bits. The address ranges are: X=0~131 (column address), Y=0~8 (page address). Addresses outside these ranges are not allowed.

7-2 Page Address Circuit

This circuit provides the page address of DDRAM. It incorporates 4-bit Page Address Register which can be modified by the “Page Address Set” instruction only. The Page Address must be set before accessing DDRAM content. Page Address “8” is a special RAM area for the icons with only one valid bit: D0.

7-3 Column Address Circuit

The column address of DDRAM is specified by the Column Address Set command. Column Address Circuit has 8-bit preset counter that provides Column Address to the Display Data RAM (DDRAM). This allows MPU accessing DDRAM content continuously. The column address is automatically incremented from the start up to the end column. During auto-increment, the column address returns to the start address as the end column (counter value) is reached.

Furthermore, Register MX and MY makes it possible to invert the relationship between the DDRAM and the outputs (COM/SEG). It is necessary to rewrite the display data into DDRAM after changing MX setting.

The relation between DDRAM and outputs with different MX or MY setting is shown below.

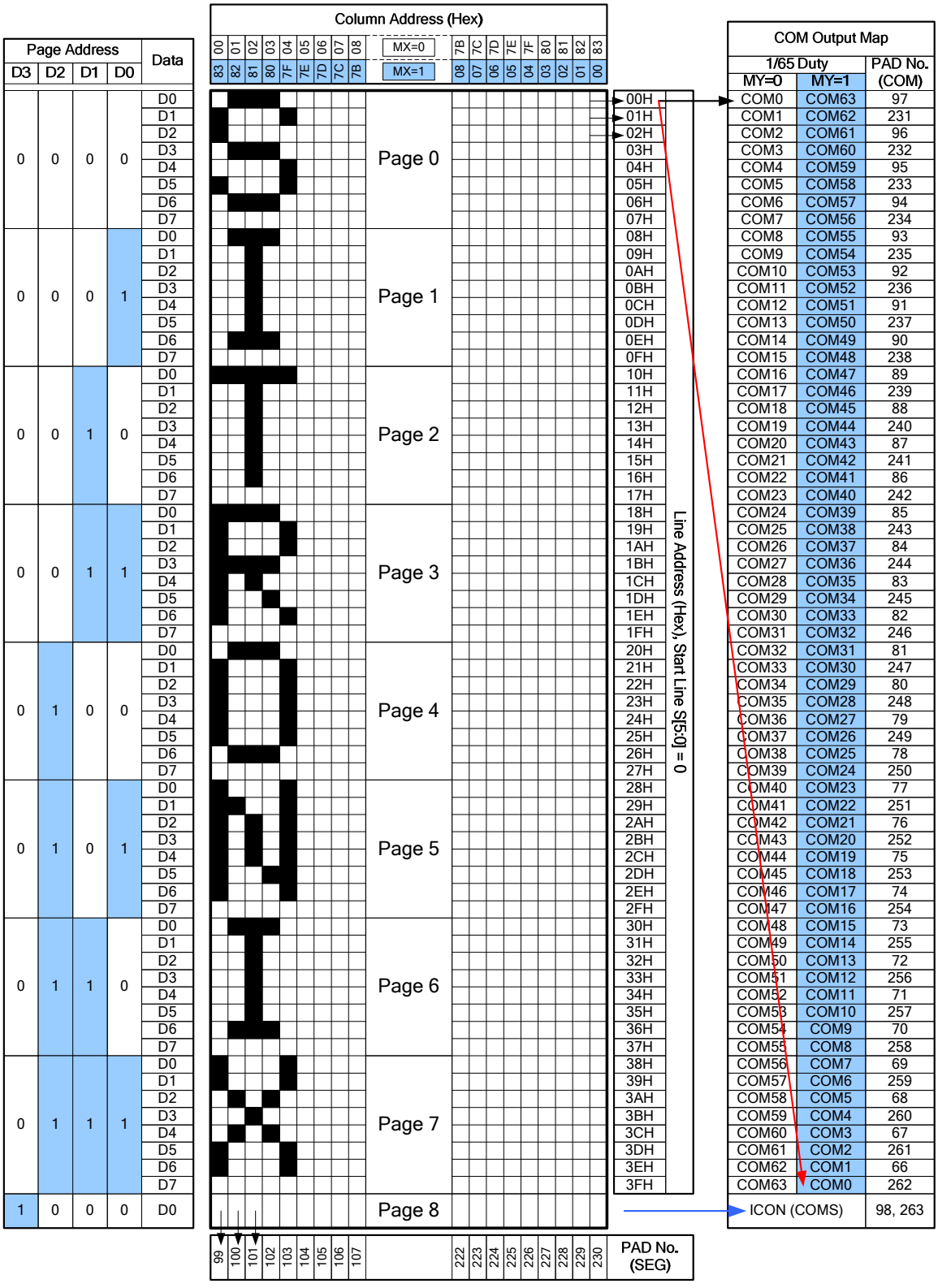


Figure 14 DDRAM and Output Map (COM/SEG) 1/65 Duty

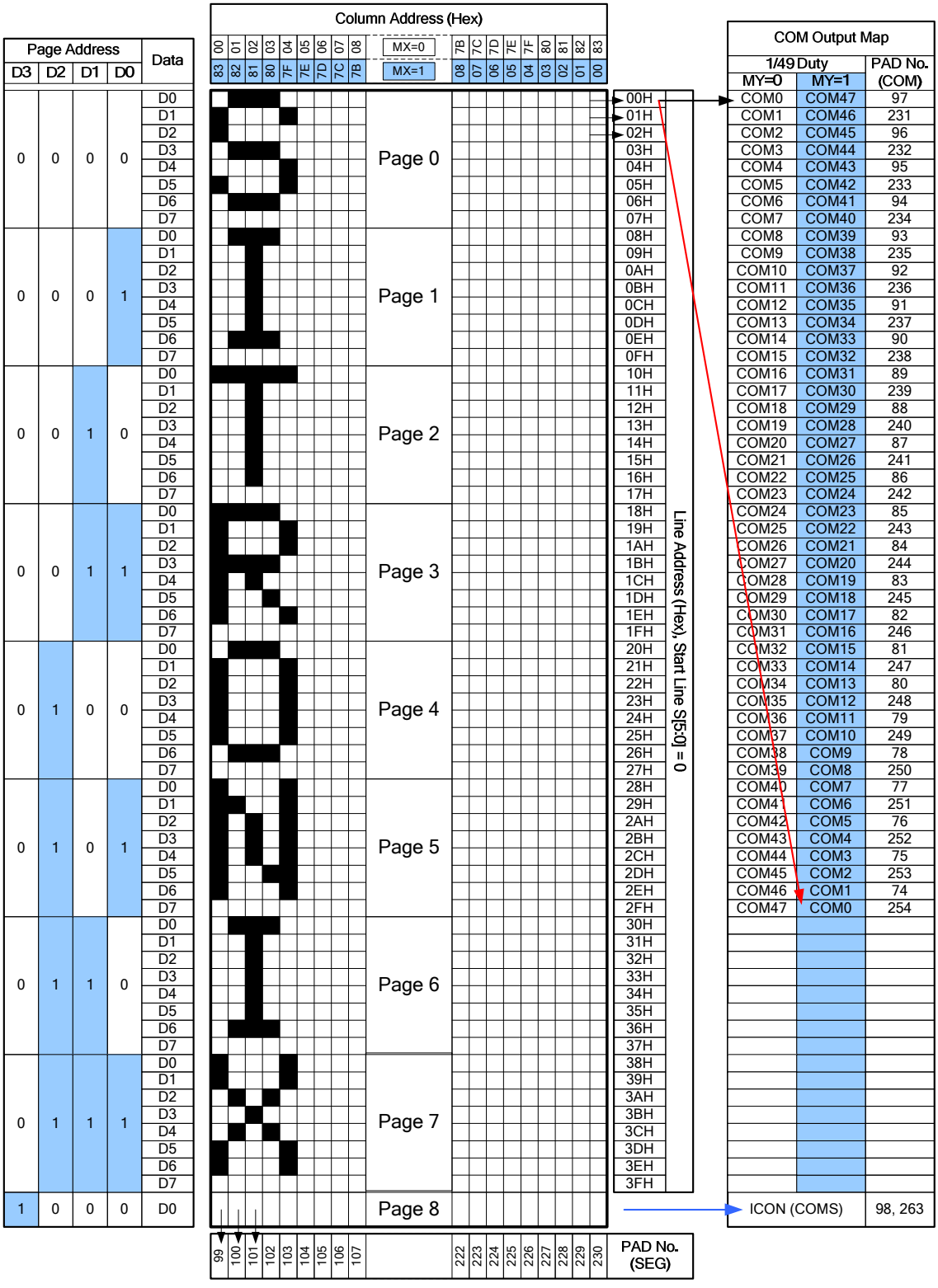


Figure 15 DDRAM and Output Map (COM/SEG) 1/49 Duty

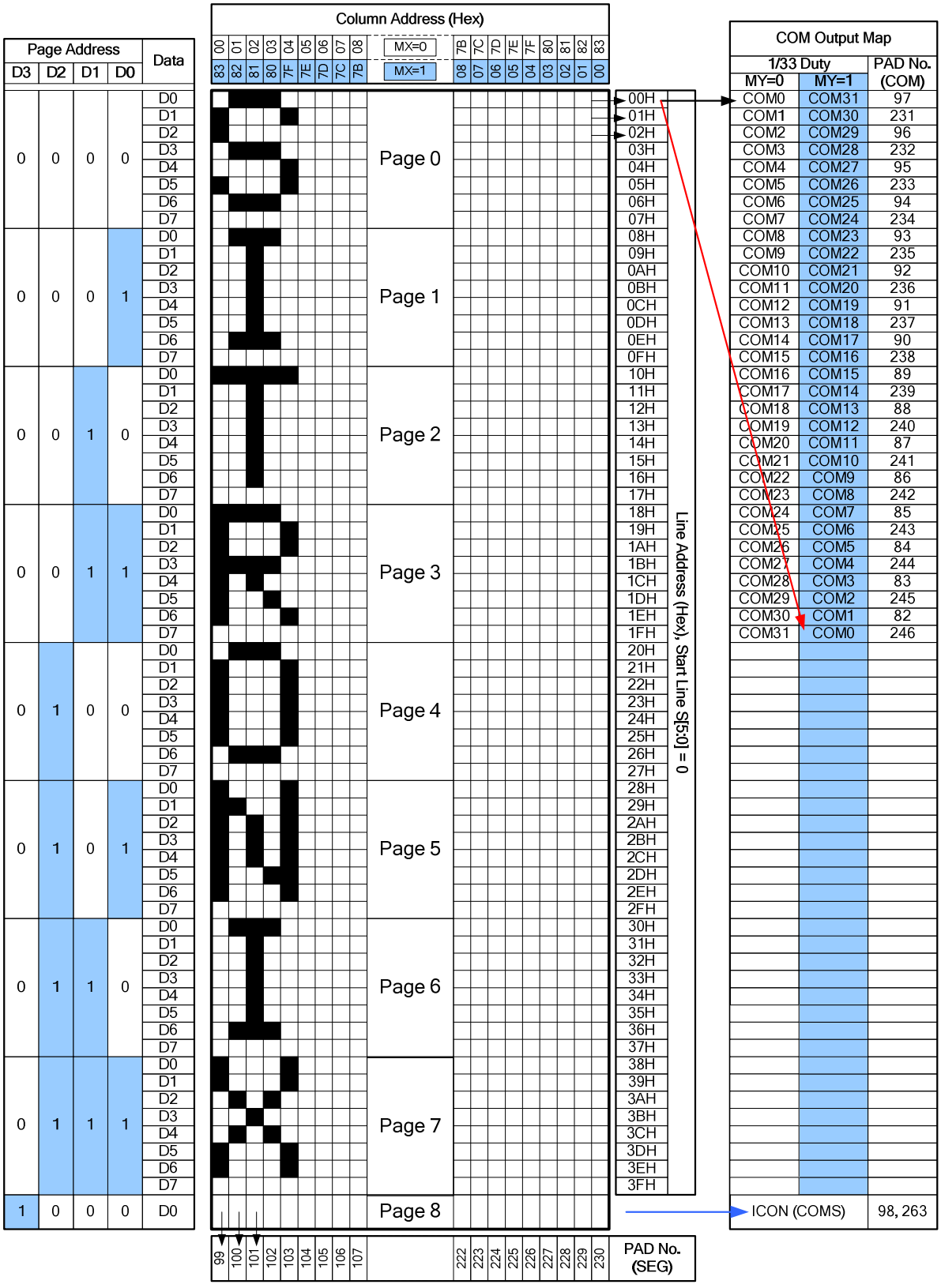


Figure 16 DDRAM and Output Map (COM/SEG) 1/33 Duty

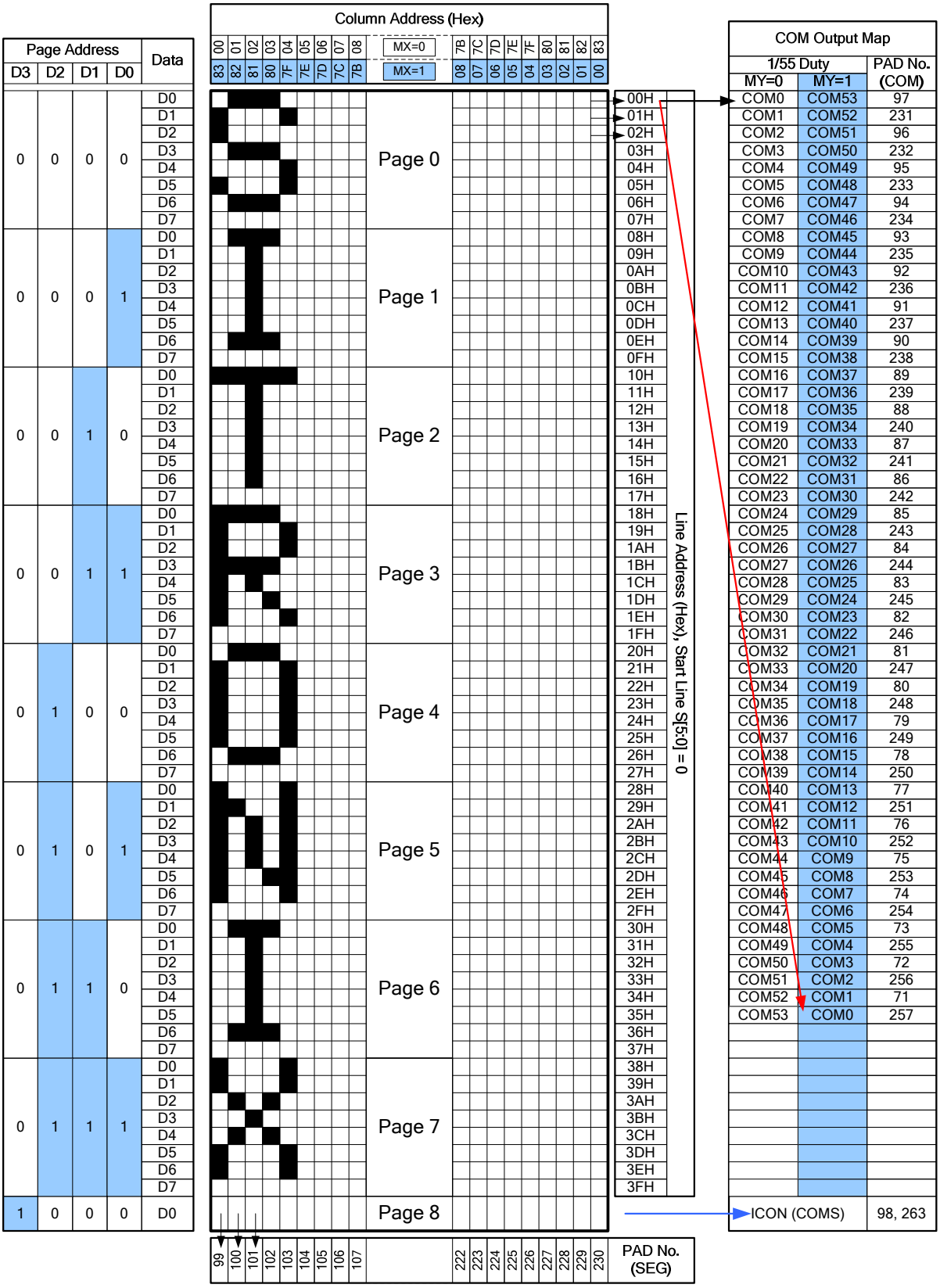


Figure 17 DDRAM and Output Map (COM/SEG) 1/55 Duty

7-4 Line Address Circuit

The Line Address Circuit incorporates a counter and a Line Address register which is changed only by the “Display Start Line Set” instruction. This circuit assigns DDRAM a Line Address corresponding to the first display line (COM0). Therefore, by setting Line Address repeatedly, ST7567S can realize the screen scrolling without changing the contents of DDRAM as shown in Fig. 18. The last common is always the COMS (common output for the icons). That means the icons will never scroll with the general display data.

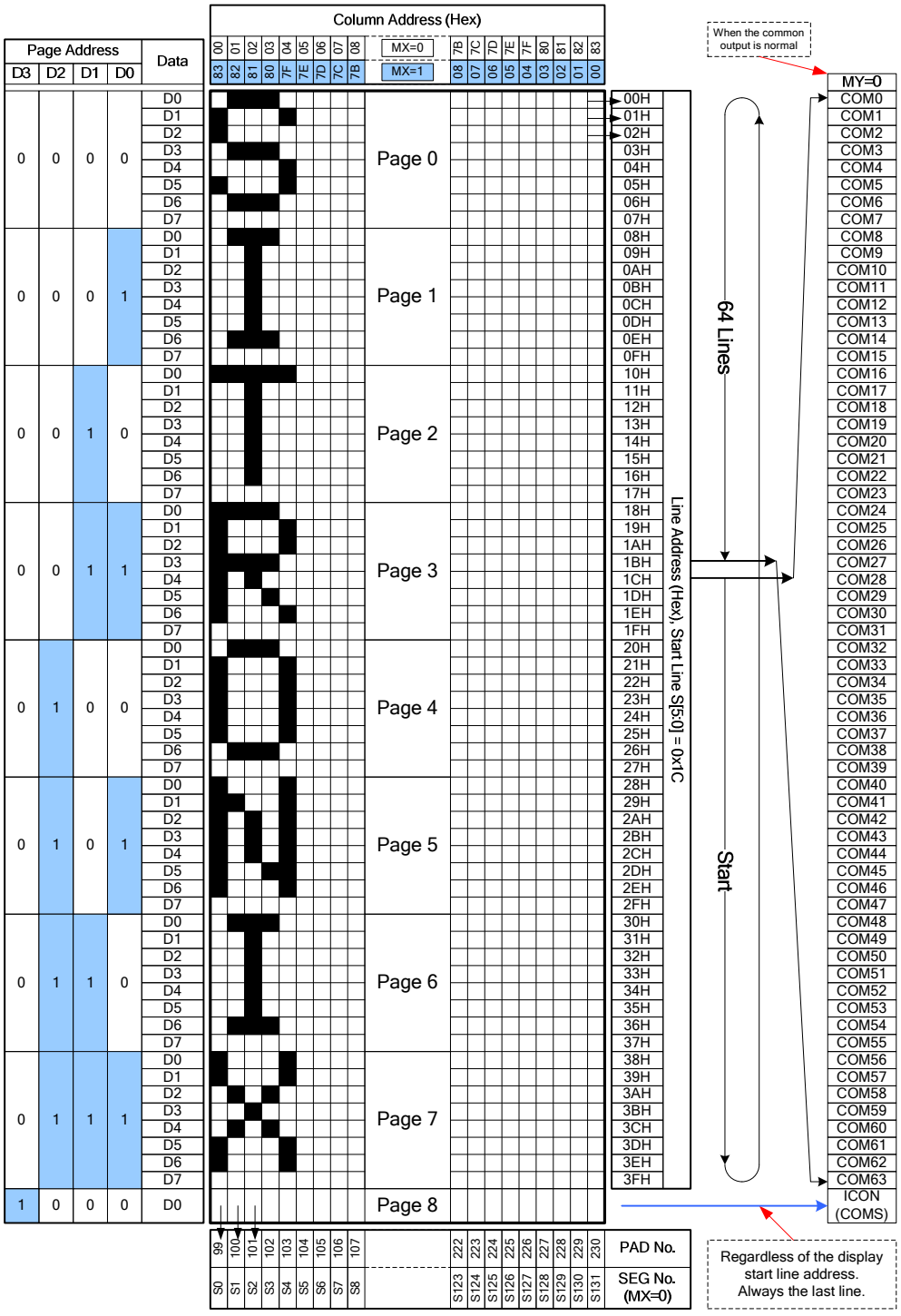


Figure 18 Start Line Function

7-5 Display Data Latch Circuit

The display data latch circuit latches temporarily display data of each segment output which will be output at the next clock. The special functions such as reverse display, display OFF and display all points ON only change the data in the latch and the content in the Display Data RAM is not changed.

7-6 Oscillation Circuit

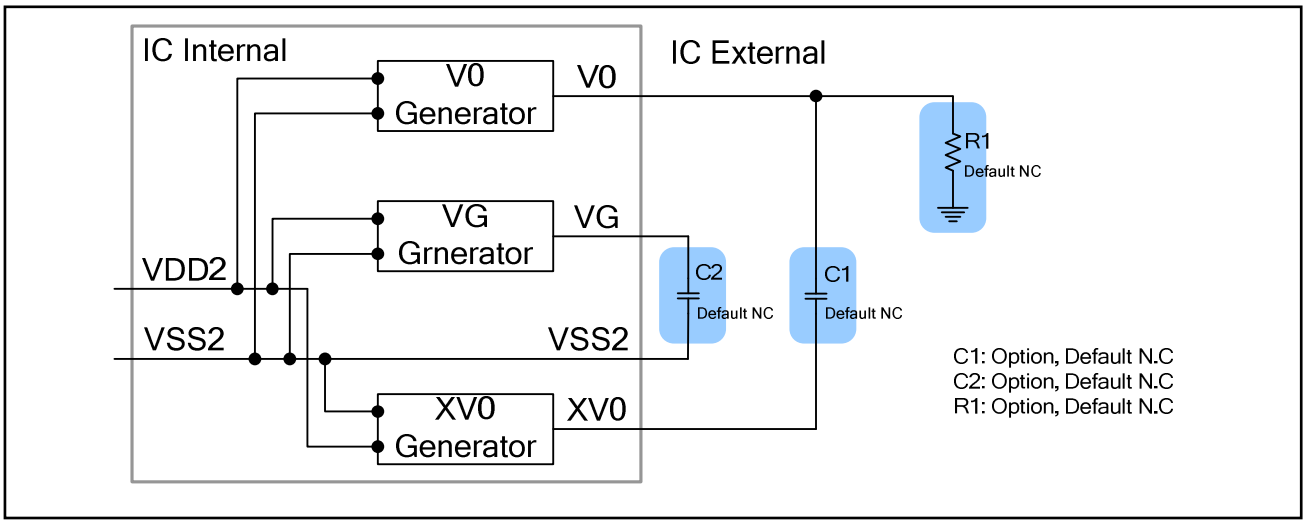
The built-in oscillation circuit generates the system clock for the liquid crystal driving circuit. The oscillation circuit is enabled after initializing ST7567S. The clock will not be output to reduce the power consumption.

7-7 Liquid Crystal Driver Power Circuit

The built-in power circuits generate the voltage levels which are necessary to drive the liquid crystal. It consumes low power with the fewest external components. The built-in power system has voltage booster, voltage regulator and voltage follower circuits. Before power ST7567S OFF, a Power OFF procedure is needed (please refer to the OPERATION FLOW section).

7-8 External Components of Power Circuit

The detailed values of these two capacitors are determined by the panel size and loading.



Components selection notes:

- If the panel size is larger than 2” or heavy loading, must be added the capacitor C1 and C2.
- If the icon is used, please add capacitors C1 and C2.
- The referential external component value:
  C1=0.1uF~1.0uF (Non-Polar/25V, default N.C.)
  C2=0.1uF~1.0uF (Non-Polar/6V, default N.C.)
  R1=500KΩ~1MΩ (default N.C.)
- Higher capacitor values are recommended for ripple reduction.
- In order to avoid the characteristic differences of the LCD panel. The capacitor values should be verified according to the display performance on LCD panel.

Regulator Circuit

The built-in high accuracy regulation circuit has 8 regulation ratios and each one has 64 EV-levels for voltage adjustment. Without additional external component, the output voltage can be changed by instructions such as “Regulation Ratio” and “Set EV”. The detailed setting method can be found in the INSTRUCTION DESCRIPTION section.

8 RESET CIRCUIT

Setting RSTB to “L” can initialize internal function. While RSTB is “L”, no instruction except read status can be accepted. RSTB pin must connect to the reset pin of MPU and initialization by RSTB pin is essential before operating. Please note the hardware reset is not same as the software reset. When RSTB becomes “L”, the hardware reset procedure will start. When RESET instruction is executed, the software reset procedure will start. The procedure is listed below:

Procedure	Hardware Reset	Software Reset
Display OFF: D=0, all SEGs/COMs output at VSS	V	X
Normal Display: INV=0, AP=0	V	X
SEG Normal Direction: MX=0	V	X
Clear Serial Counter and Shift Register (if using Serial Interface)	V	X
Bias Selection: BS=0	V	X
Booster Level BL=0	V	X
Exit Power Saving Mode	V	X
Power Control OFF: VB=0, VR=0, VF=0	V	X
Exit Read-modify-Write mode	V	V
Start Line S[5:0]=0	V	V
Column Address X[7:0]=0	V	V
Page Address Y[3:0]=0	V	V
COM Normal Direction: MY=0	V	V
V0 Regulation Ratio RR[2:0]=(1,0,0)	V	V
EV[5:0]=(1,0,0,0,0,0)	V	V

After power-on, RAM data are undefined and the display status is “Display OFF”. It’s better to initialize whole DDRAM (ex: fill all 00h or write the display pattern) before turning the Display ON. Besides, the power is not stable at the time that the power is just turned ON. A hardware reset is needed to initialize those internal registers after the power is stable.

9 INSTRUCTION

9-1 INSTRUCTION TABLE

INSTRUCTION	A0	R/W (RWR)	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
(1) Display ON/OFF	0	0	1	0	1	0	1	1	1	D	D=1, display ON D=0, display OFF
(2) Set Start Line	0	0	0	1	S5	S4	S3	S2	S1	S0	Set display start line
(3) Set Page Address	0	0	1	0	1	1	Y3	Y2	Y1	Y0	Set page address
(4)Set Column Address	0	0	0	0	0	1	X7	X6	X5	X4	Set column address (MSB)
	0	0	0	0	0	0	X3	X2	X1	X0	Set column address (LSB)
(5) Read Status	0	1	0	MX	D	RST	0	0	0	0	Read IC Status
(6) Write Data	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write display data to RAM
(7) Read Data	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read display data from RAM
(8) SEG Direction	0	0	1	0	1	0	0	0	0	MX	Set scan direction of SEG MX=1, reverse direction MX=0, normal direction
(9) Inverse Display	0	0	1	0	1	0	0	1	1	INV	INV =1, inverse display INV =0, normal display
(10) All Pixel ON	0	0	1	0	1	0	0	1	0	AP	AP=1, set all pixel ON AP=0, normal display
(11) Bias Select	0	0	1	0	1	0	0	0	1	BS	Select bias setting 0=1/9; 1=1/7 (at 1/65 duty)
(12) Read-modify-Write	0	0	1	1	1	0	0	0	0	0	Column address increment: Read:+0 , Write:+1
(13) END	0	0	1	1	1	0	1	1	1	0	Exit Read-modify-Write mode
(14) RESET	0	0	1	1	1	0	0	0	1	0	Software reset
(15) COM Direction	0	0	1	1	0	0	MY	-	-	-	Set output direction of COM MY=1, reverse direction MY=0, normal direction
(16) Power Control	0	0	0	0	1	0	1	VB	VR	VF	Control built-in power circuit ON/OFF
(17) Regulation Ratio	0	0	0	0	1	0	0	RR2	RR1	RR0	Select regulation resistor ratio
(18) Set EV	0	0	1	0	0	0	0	0	0	1	Double command!! Set electronic volume (EV) level
	0	0	0	0	EV5	EV4	EV3	EV2	EV1	EV0	
(19) Set Booster	0	0	1	1	1	1	1	0	0	0	Double command!! Set booster level: BL=0: 4X BL=1: 5X
	0	0	0	0	0	0	0	0	0	BL	
(20) Power Save	0	0	Compound Command								Display OFF + All Pixel ON
(21) NOP	0	0	1	1	1	0	0	0	1	1	No operation
(22) SPI Read Status	0	1	1	1	1	1	1	1	0	0	SPI read status command
	0	1	0	MX	D	RST	ID3	ID2	ID1	ID0	
(23) SPI Read DDRAM	0	1	1	1	1	1	1	1	0	1	SPI read DDRAM command
	1	1	D7	D6	D5	D4	D3	D2	D1	D0	

Note: Symbol “-” means this bit can be “H” or “L”.

9-2 INSTRUCTION DESCRIPTION

9-2-1 Display ON/OFF

The D flag selects the display mode.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	1	1	1	D

D=1: Normal Display Mode.

D=0: Display OFF. All SEGs/COMs output with VSS.

9-2-2 Set Start Line

This instruction sets the line address of the Display Data RAM to determine the initial display line. The display data of the specified line address is displayed at the top row (COM0) of the LCD panel.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	S5	S4	S3	S2	S1	S0

S5	S4	S3	S2	S1	S0	Line address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
0	0	0	0	1	1	3
:	:	:	:	:	:	:
1	1	1	1	0	1	61
1	1	1	1	1	0	62
1	1	1	1	1	1	63

9-2-3 Set Page Address

Y [3:0] defines the Y address vector address of the display RAM.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	1	Y3	Y2	Y1	Y0

Y3	Y2	Y1	Y0	Page Address	Valid Bit
0	0	0	0	Page0	D0~ D7
0	0	0	1	Page1	D0~ D7
0	0	1	0	Page2	D0~ D7
:	:	:	:	:	:
0	1	1	0	Page6	D0~ D7
0	1	1	1	Page7	D0~ D7
1	0	0	0	Page8 (icon page)	D0

9-2-4 Set Column Address

This instruction is used to define area of DDRAM where MCU can access. The column address is automatically increased by one after each byte of display data access (read/write). The X[7:0] setting that must be less than or equal to “83h”. If X[7:0] setting is great than 83h, out of DDRAM range will be ignored.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	X7	X6	X5	X4

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	X3	X2	X1	X0

X7	X6	X5	X4	X3	X2	X1	X0	Column Address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	1	1	3
:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	0	1	129
1	0	0	0	0	0	1	0	120
1	0	0	0	0	0	1	1	131

9-2-5 Read Status

Read the internal status of ST7567S. The read function is not available in serial interface mode.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	MX	D	RST	0	0	0	0

Flag	Description
MX	MX=0: Normal direction (SEG0->SEG131) MX=1: Reverse direction (SEG131->SEG0)
D	D=0: Display ON D=1: Display OFF
RST	RST=1: During reset (hardware or software reset) RST=0: Normal operation

9-2-6 Write Data

8-bit data of Display Data from the microprocessor can be written to the RAM location specified by the column address and page address. The column address is increased by 1 automatically so that the microprocessor can continuously write data to the addressed page. During auto-increment, the column address wraps to 0 after the last column is written.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
1	0	Write Data							

9-2-7 Read Data

8-bit data of Display Data from the RAM location specified by the column address and page address can be read to the microprocessor.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
1	1	Read Data							

9-2-8 SEG Direction

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	0	0	0	MX

Flag	Description
MX	MX=0: Normal direction (SEG0->SEG131) MX=1: Reverse direction (SEG131->SEG0)

9-2-9 Inverse Display

This instruction changes the selected and non-selected voltage of SEG. The display will be inversed (White -> Black, Black -> White) while the display data in the Display Data RAM is never changed.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	0	1	1	INV

Flag	Description
INV	INV=0: Normal display INV =1: Inverse display

9-2-10 All Pixel ON

This instruction will let all segments output the selected voltage and make all pixels turned ON.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	0	1	0	AP

Flag	Description
AP	AP =0: Normal display AP =1: All pixels ON

9-2-11 Bias Select

Select LCD bias ratio of the voltage required for driving the LCD.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	0	0	1	BS

Duty	Bias	
	BS=0	BS=1
1/65	1/9	1/7
1/49	1/8	1/6
1/33	1/6	1/5
1/55	1/8	1/6

Reference LCD Bias Voltage (1/65 Duty with 1/9 Bias)

Symbol	Bias Voltage
V0	V0
VG	2/9 x V0
VM	1/9 x V0
VSS	VSS

Please Note:

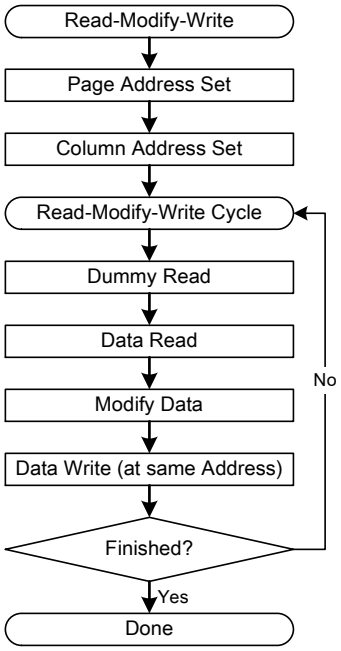
* VG range: 1.6V ≤ VG < VDD2-0.2V.
* VM range: 0.8V ≤ VM < VG.

9-2-12 Read-modify-Write

This command is used paired with the “END” instruction. Once this command has been input, the display data read operation will not change the column address, but only the display data write operation will increase the column address (X[7:0]+1). This mode is maintained until the END command is input. This function makes it possible to reduce the load on the MPU when there are repeating data changes in a specified display region, such as a blanking cursor.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	0	0	0	0	0

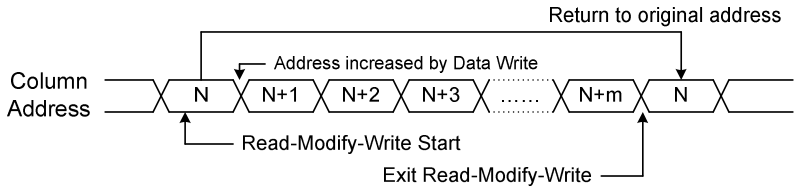
⇨ In Read-modify-Write mode, other instructions aside from display data read/write commands can also be used.



9-2-13 END

When the END command is input, the Read-modify-Write mode is released and the column address returns to the address it was when the Read-modify-Write instruction was entered.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	0	1	1	1	0



9-2-14 RESET

This instruction resets Start Line (S[5:0]), Column Address (X[7:0]), Page Address (Y[3:0]) and COM Direction (MY) to their default setting. Please note this instruction is not complete same as hardware reset (RSTB=L) and cannot initialize the built-in power circuit which is initialized by the RSTB pin. The detailed information is in “Section 8 Reset Circuit”.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	0	0	0	1	0

9-2-15 COM Direction

This instruction controls the common output status which changes the vertical display direction. The detailed information can be found in Fig 14~17.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	0	0	MY	-	-	-

Flag	Description
MY	MY=0: Normal direction (COM0->COM63) MY=1: Reverse direction (COM63->COM0)

9-2-16 Power Control

This instruction controls the built-in power circuits. Typically, these 3 flags are turned ON at the same time.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	1	VB	VR	VF

Flag	Description
VB	VB=0: Built-in Booster OFF VB=1: Built-in Booster ON
VR	VR=0: Built-in Regulator OFF VR=1: Built-in Regulator ON
VF	VF=0: Built-in Follower OFF VF=1: Built-in Follower ON

9-2-17 Regulation Ratio

This instruction controls the regulation ratio of the built-in regulator.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	0	RR2	RR1	RR0

RR2	RR1	RR0	Regulation Ratio (RR)
0	0	0	3.0
0	0	1	3.5
0	1	0	4.0
0	1	1	4.5
1	0	0	5.0
1	0	1	5.5
1	1	0	6.0
1	1	1	6.5

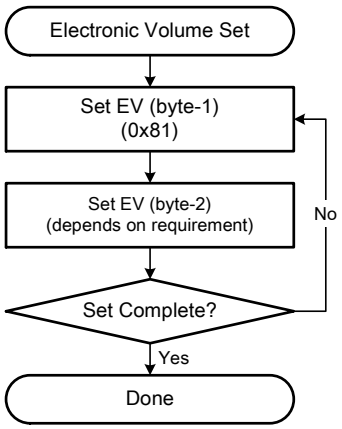
The operation voltage (V0) calculation formula is shown below: (RR comes from Regulation Ratio, EV comes from EV[5:0])
V0 = RR X [1 – (63 – EV) / 162] X 2.1, or **V0 = RR X [(99 + EV) / 162] X 2.1**

SYMBOL	REGISTER	VALUE
RR	RR[2:0]	3.0, 3.5, 4.0, 4.5, 5.0, 5.5, 6.0 and 6.5
EV	EV[5:0]	0~63

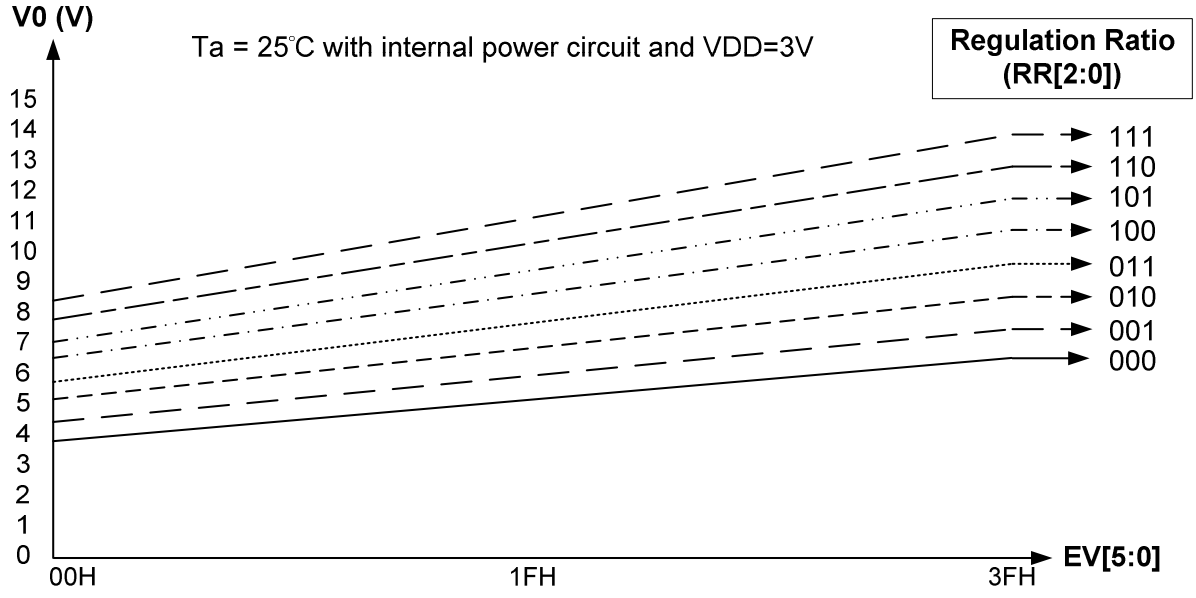
9-2-18 Set EV

This is double byte instruction. The first byte set ST7567S into EV adjust mode and the following instruction will change the EV setting. That means these 2 bytes must be used together. They control the electronic volume to adjust a suitable V0 voltage for the LCD.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	0	0	0	0	0	1
0	0	0	0	EV5	EV4	EV3	EV2	EV1	EV0



The maximum voltage that can be generated is dependent on the VDD2 voltage and the loading of LCD module. There are 8 V0 voltage curve can be selected. It is recommended the EV should be close to the center (1FH) for easy contrast adjustment.

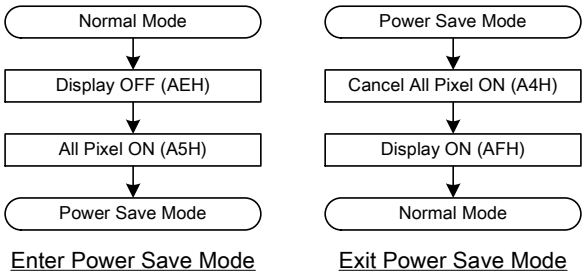


EV[5:0] and RR[2:0] vs. V0 Voltage

9-2-19 Power Save(Compound Instruction)

This is compound instruction. The 1st instruction is Display OFF (D=0) and the 2nd instruction is All Pixel ON (AP=1). The Power Save mode starts the following procedure: (the display data and register settings are still kept except D-Flag and AP-Flag)

1. Stops internal oscillation circuit;
2. Stops the built-in power circuits;
3. Stops the LCD driving circuits and keeps the common and segment outputs at VSS.



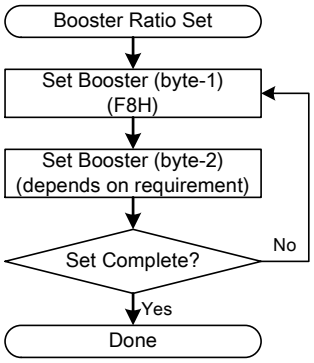
After exiting Power Save mode, the settings will return to be as they were before.

9-2-20 Set Booster

This is double byte instruction. The first byte set ST7567S into booster configuration mode and the following instruction will change the booster setting. That means these 2 bytes must be used together. They control the built-in booster circuit to provide the power source of the built-in regulator. ST7567S booster is built-in booster capacitors. Booster level can be changed with instruction only without changing hardware connection.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	1	1	0	0	0
0	0	0	0	0	0	0	0	0	BL

BL	Boost Level
0	X4
1	X5



9-2-21 NOP

“No Operation” instruction. ST7567S will do nothing when receiving this instruction.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	0	0	0	1	1

9-2-22 SPI Read Status

Indicate the status of read by 3-Line and 4-Line SPI

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	1	1	1	1	0	0
0	1	0	MX	D	RST	ID3	ID2	ID1	ID0

9-2-23 SPI Read DDRAM

8-bit data of Display Data from the RAM location specified by the column address and page address can be read to the microprocessor.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	1	1	1	1	0	1
1	1	D7	D6	D5	D4	D3	D2	D1	D0

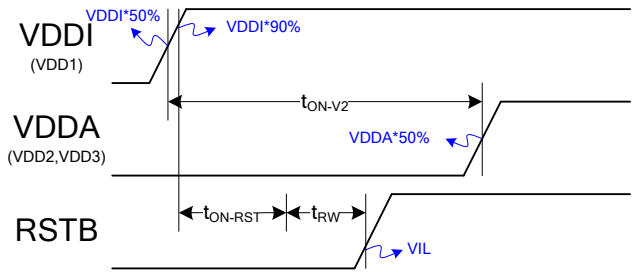
10. OPERATION FLOW

This section introduces some reference operation flows.

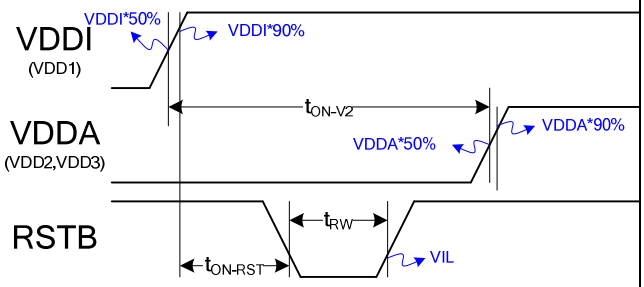
10-1Power ON Sequence

Operation Sequence

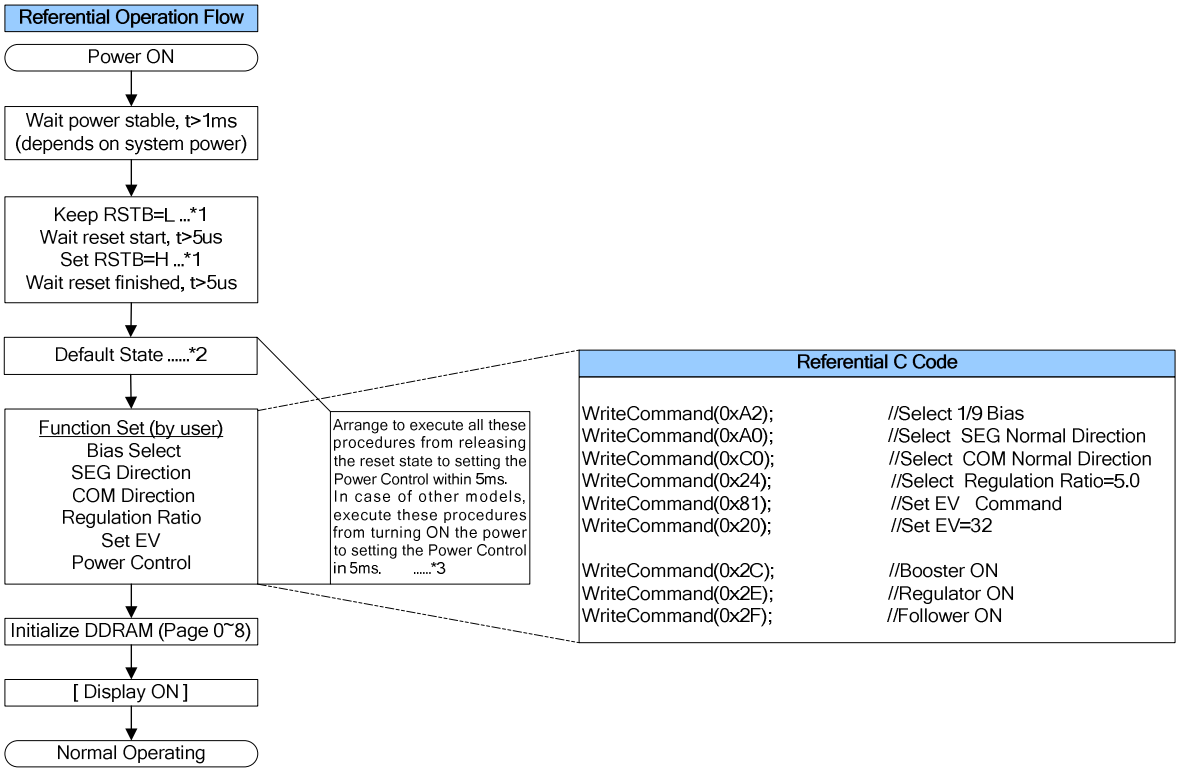
Case 1: RSTB=L while Power ON



Case 2: RSTB=H while Power ON



Power ON Operation Flow



Note: The detailed description can be found in the respective sections listed below.

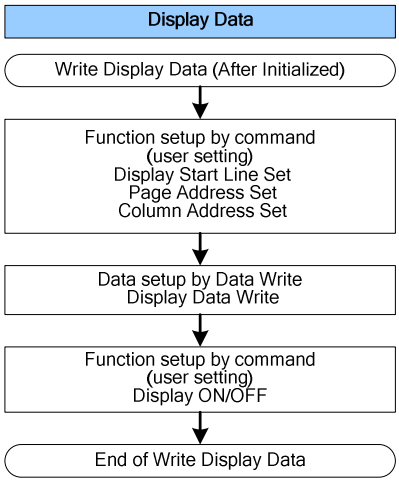
1. Please refer to the timing specification of t_{RW} and t_R.
2. Refer to Section 8 Reset Circuit.
3. The 5ms requirement depends on the characteristics of LCD panel and the external component of the power circuit. It is recommended to check with the real products with external component.
4. The detailed instruction functionality is described in Section 9-2 INSTRUCTION INTRODUCTION;
5. Power stable is defined as the time that the later power (VDDI or VDDA) reaches 90% of its rated voltage.

Timing Requirement:

Item	Symbol	Requirement	Note
VDDA power delay	t_{ON-V2}	$0 \le t_{ON-V2}$	● Applying VDDI and VDDA in any order will not damage IC.
RSTB input time	t_{ON-RST}	No Limitation	● If RSTB is Low, High or unstable during power ON, a successful hardware reset by RSTB is required after VDDI is stable. ● RSTB=L can be input at any time after power is stable. ● t_{RW} & t_R should match the timing specification of RSTB. ● To prevent abnormal display, the recommended timing is: 1ms ≤ t_{ON-RST} ≤ 30 ms.

- The requirement listed here is to prevent abnormal display on LCD module.

10-2 Display Data



Reference C Code

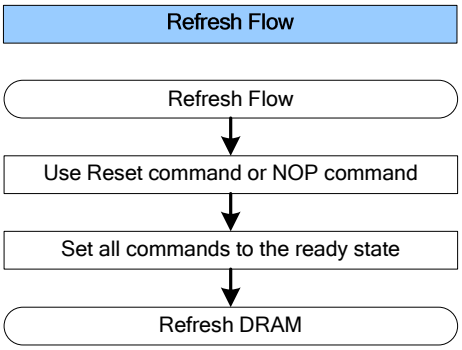
```
Extern unsigned char picture[8][132];                    //Picture must be set
Void WriteDisplayData(void)
{
  int page=0, column=0;                                  //Picture data
  int pageAddr=0xB0;                                     //Set page=page0

  WriteCommand(0x40);                                    //Set start line address=0x00

  for( page=0; page<9; page++)                           //Send picture data
  {                                                     //From page 0 to page 8
     WriteCommand(pageAddr);                             //Set Page
     WriteCommand(0x10);                                 //Set MSB Column address
     WriteCommand(0x00);                                 //Set LSB Column address
     for( column=0; column<132; column++)                //Send picture data
     {                                                  //From column 0 to column 132
          WriteData(picture[page][column]);              //Write picture data
     }
        pageAddr++;                                     //Set page= next page
  }
}
   WriteCommand(0xAF);                                   //Display ON(0xAF)
```

Notes: Reference items

1. The detailed instruction functionality is described in Section 9-2 INSTRUCTION DESCRIPTION;
2. It is recommended to write display data (initialize DDRAM) before Display ON.

10-3 Refresh

It is recommended to use the refresh sequence regularly in a specified interval.

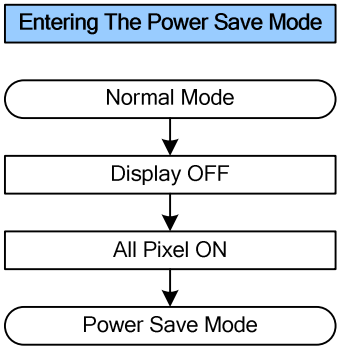


Use Reset command or NOP command

```
WriteCommand(0xE2):          //SoftwareReset
          or
WriteCommand(0xE3):          //NOP

WriteCommand(0xA2);          //Select 1/9Bias
WriteCommand(0xA0);          //Select SEG Normal Direction
WriteCommand(0xC0);          //Select COM Normal Direction
WriteCommand(0x24);          //Select Regulation Ratio=5.0
WriteCommand(0x81);          //Set EV Command
WriteCommand(0x20);          //Set EV=32

WriteCommand(0x2C);          //Booster ON
WriteCommand(0x2E);          //Regulator ON
WriteCommand(0x2F);          //Follower ON

WriteDisplayData();          //WriteDisplayData
```

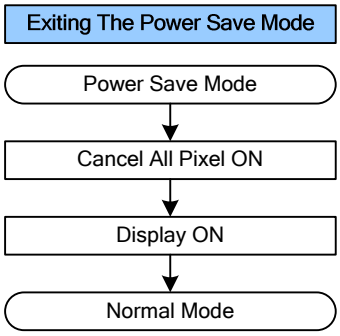
10-4 Power-Save Flow and Sequence

Entering the Power Save Mode:



Reference C Code	
WriteCommand (0xAE);	//Display OFF
WriteCommand (0xA5);	//All Pixel ON

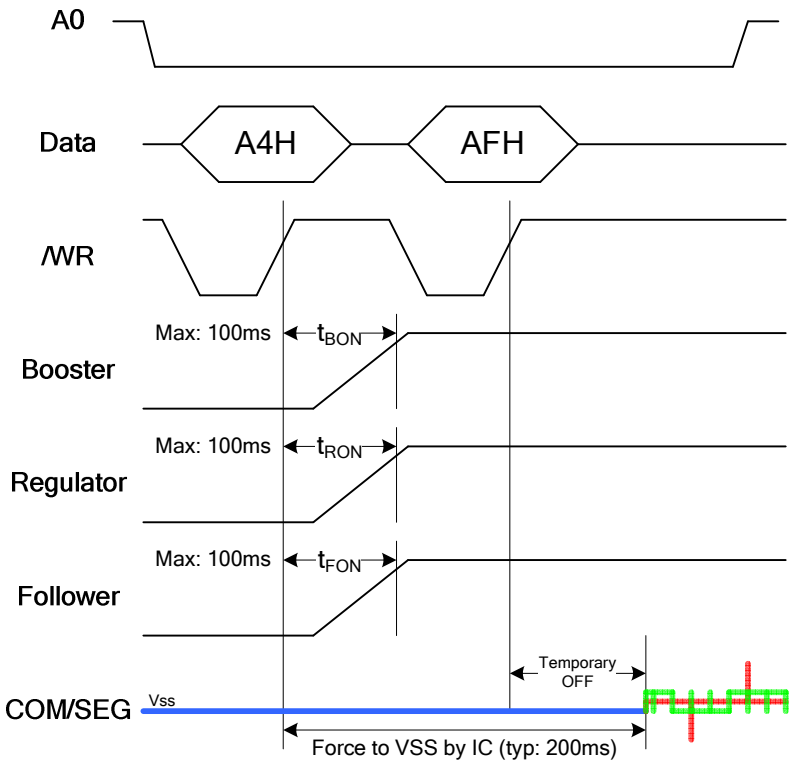
Exiting the Power Save Mode:



Reference C Code	
WriteCommand(0xA4);	//Cancel All Pixel ON
WriteCommand(0xAF);	//Display ON

INTERNAL SEQUENCE of EXIT POWER SAVE MODE

After receiving power save instruction, the internal circuits (Power) will starts the following procedure.

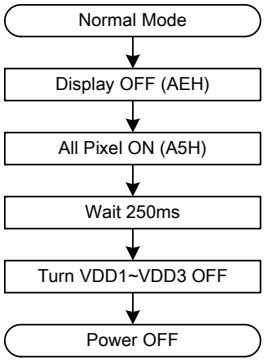
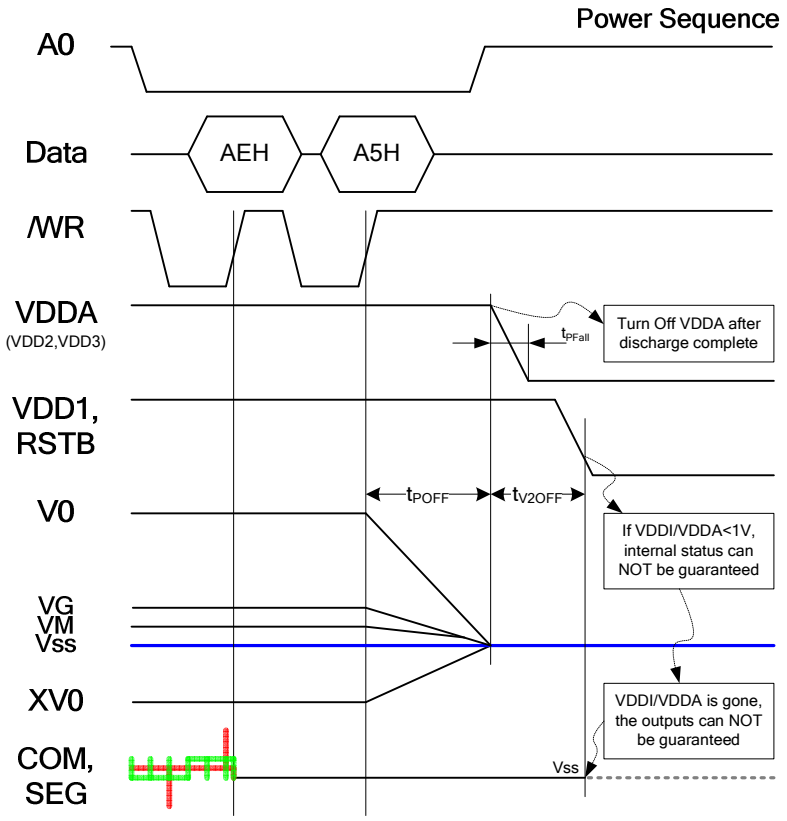
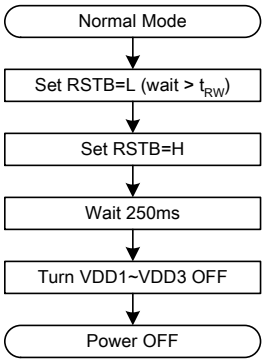
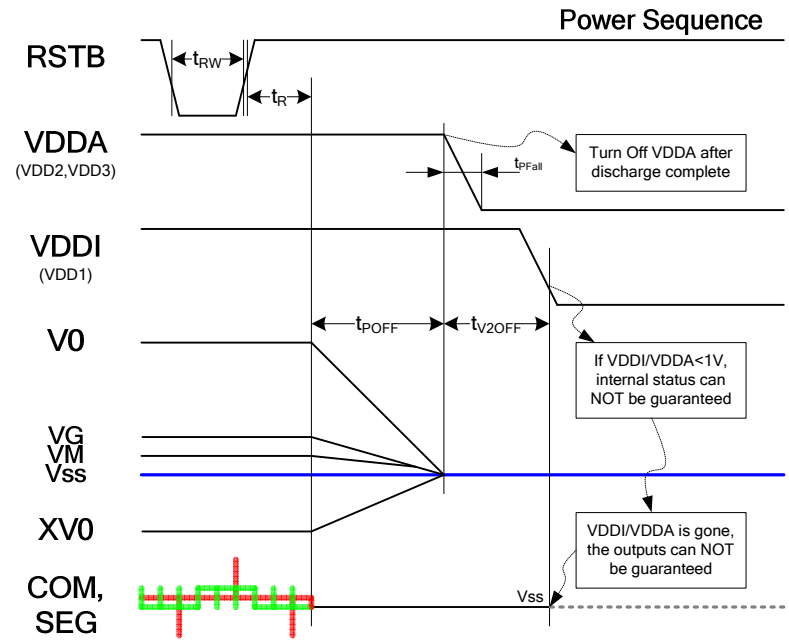


Note:

1. The power stable time is determined by LCD panel loading.
2. The power stable time in this figure is base on: LCD Panel Size = 1.4” without capacitor (VDD=2.7V, Vop=9V).

10-5 Power OFF Flow and Sequence

In power save mode, LCD outputs are fixed to VSS and all analog outputs are discharged. The power can be turned OFF after ST7567S is in the power save mode. The power save mode can be triggered by the following two methods.

Referential Power OFF Flow	Operation Sequence
CASE 1: Use Power Save Instruction	
 Power OFF Flow After the built-in power circuits are OFF and completely discharged, the power (VDDI, VDDA) can be removed.	
CASE 2: Use Hardware Reset Function	
 Power OFF Flow After the built-in power circuits are OFF and completely discharged, the power (VDDI, VDDA) can be removed.	

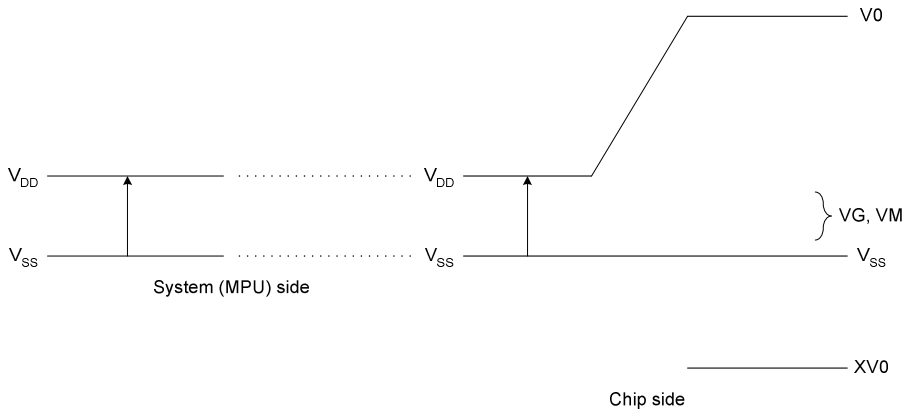
Note:

1. t_{POFF}: Internal Power discharge time. => 250ms (max).
2. t_{V2OFF}: Period between VDDI and VDDA OFF time. => 0 ms (min).
3. It is NOT recommended to turn VDDI OFF before VDDA. Without VDDI, the internal status cannot be guaranteed and internal discharge-process maybe stopped. The un-discharged power maybe flows into COM/SEG output(s) and the liquid crystal in panel maybe polarized.
4. IC will NOT be damaged if either VDDI or VDDA is OFF while another is ON.
5. The timing is dependent on panel loading and the external capacitor(s).
6. The timing in these figures is base on the condition that: LCD Panel Size = 1.4” without capacitor.
7. When turning VDDA OFF, the falling time should follow the specification: 20ms ≤ t_{Pfall} ≤ 0.2sec

11 LIMITING VALUES

In accordance with the Absolute Maximum Rating System; please refer to notes 1 and 2.

Parameter	Symbol	Conditions	Unit
Digital Power Supply Voltage	VDD1	-0.3 ~ 4.0	V
Analog Power supply voltage	VDD2, VDD3	-0.3 ~ 4.0	V
Input Voltage	VIN	-0.3 ~ VDD1+0.3	V
Operating temperature	TOPR	-30 to +85	˚C
Storage temperature	TSTR	-55 to +125	˚C
LCD power supply voltage	V0-XV0	-0.3~14	V
LCD power supply voltage	VG	-0.3~3.6	V



Notes

1. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to VSS unless otherwise noted.
2. That the stress exceeds the Limiting Value listed above it may cause the driver IC permanent damage. These values are for stress only. IC should be operated under the DC/Timing Characteristic conditions for normal operation. If these conditions are not met, IC operation may be error and the reliability may be deteriorated.
3. Insure the voltage levels of V0, VDD2, VG, VM, VSS and XV0 always match the correct relation:
   V0 ≥ VDD2 > VG > VM > VSS ≥ XV0
4. VIN should be less than or equal to 3.6V. (VIN ≤ 3.6V)

12 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

13 DC CHARACTERISTICS

VSS=0V; Temp=-30˚C to +85˚C; unless otherwise specified.

Item	Symbol	Condition	Rating			Unit	Applicable Pin
			Min.	Typ.	Max.		
Operating Voltage (1)	VDD1		1.7	—	3.6	V	VDD1
Operating Voltage (2)	VDD2		2.4	—	3.6	V	VDD2
Operating Voltage (3)	VDD3		2.4	—	3.6	V	VDD3
Input High-level Voltage	V_{IHC}		0.7 x VDD1	—	VDD1	V	MPU Interface
Input Low-level Voltage	V_{ILC}		VSS1	—	0.3 x VDD1	V	MPU Interface
Output High-level Voltage	V_{OHC}	I_{OUT}=1mA, VDD1=1.8V	0.8 x VDD1	—	VDD1	V	D[7:0]
Output Low-level Voltage	V_{OLC}	I_{OUT}=-1mA, VDD1=1.8V	VSS1	—	0.2 x VDD1	V	D[7:0]
Input Leakage Current	I_{LI}		−1.0	—	1.0	μA	MPU Interface
Output Leakage Current	I_{LO}		−3.0	—	3.0	μA	MPU Interface
Liquid Crystal Driver ON Resistance	R_{ON}	Ta=25˚C, Vop=8.5V, △V=0.85V	—	0.6	0.8	KΩ	COMx
		Ta=25˚C, VG=1.9V △V=0.19V	—	1.3	1.5	KΩ	SEGx
Frame Frequency	FR	Duty=1/65, Vop=8.5V Ta = 25℃	70	75	80	Hz	
LCD Power Supply Voltage	VLCD	Ta = 25℃	4.0	—	13	V	V0-XV0

Current consumption: During Display, with internal power system, current consumed by whole IC (bare die).

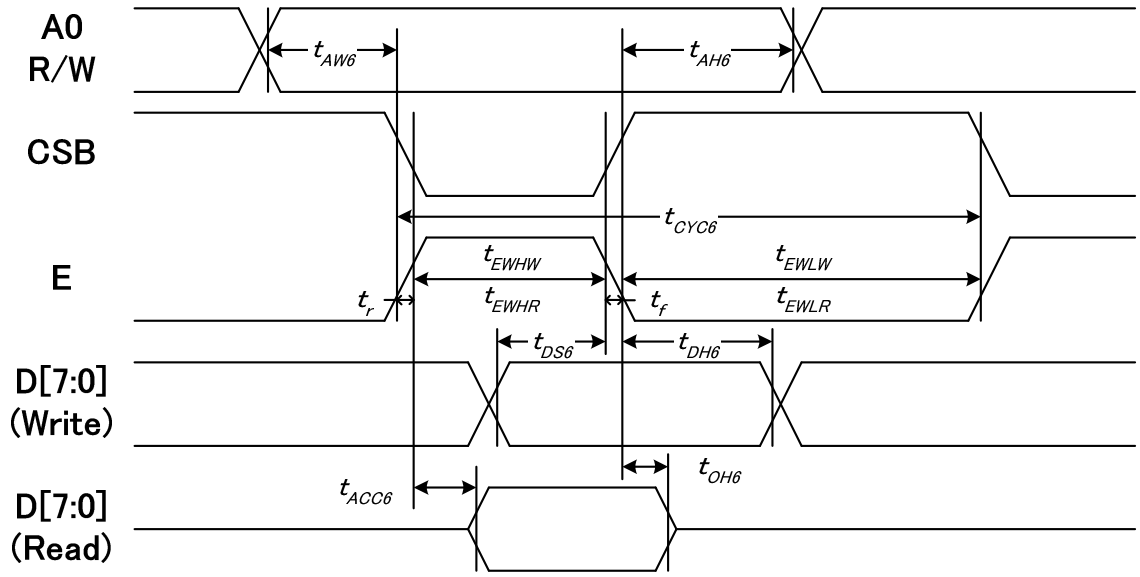
Test Pattern	Symbol	Condition	Rating			Unit	Note
			Min.	Typ.	Max.		
Display Pattern: SNOW (Static)	ISS	VDD1=VDD2=VDD3=3.0V, Booster X5 V_{OP} = 8.5 V, Bias=1/9 Ta=25˚C	—	150	300	μA	
Display OFF	ISS	VDD1=VDD2=VDD3=3.0V, Booster X5 V_{OP} = 8.5 V, Bias=1/9 Ta=25˚C	—	95	190	uA	
Power Down	ISS	VDD1=VDD2=VDD3=3.0V, Ta=25˚C	—	—	4.0	μA	

Note:

The Current Consumption is DC characteristics

14 TIMING CHARACTERISTICS

14-1 System Bus Timing for 6800 Series MPU



(VDD1 = 3.3V , Ta =25˚C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW6		0	—	ns
Address hold time		tAH6		10	—	
System cycle time	E	tCYC6		240	—	
Enable L pulse width (WRITE)		tEWLW		80	—	
Enable H pulse width (WRITE)		tEWHW		80	—	
Enable L pulse width (READ)		tEWLR		80	—	
Enable H pulse width (READ)		tEWHR		140	—	
Write data setup time	D[7:0]	tDS6		40	—	
Write data hold time		tDH6		10	—	
Read data access time		tACC6	CL = 16 pF	—	70	
Read data output disable time		tOH6	CL = 16 pF	5	50	

(VDD1 = 2.8V , Ta =25˚C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW6		0	—	ns
Address hold time		tAH6		0	—	
System cycle time	E	tCYC6		400	—	
Enable L pulse width (WRITE)		tEWLW		220	—	
Enable H pulse width (WRITE)		tEWHW		180	—	
Enable L pulse width (READ)		tEWLR		220	—	
Enable H pulse width (READ)		tEWHR		180	—	
Write data setup time	D[7:0]	tDS6		40	—	
Write data hold time		tDH6		20	—	
Read data access time		tACC6	CL = 16 pF	—	140	
Read data output disable time		tOH6	CL = 16 pF	10	100	

(VDD1 = 1.8V , Ta =25˚C)

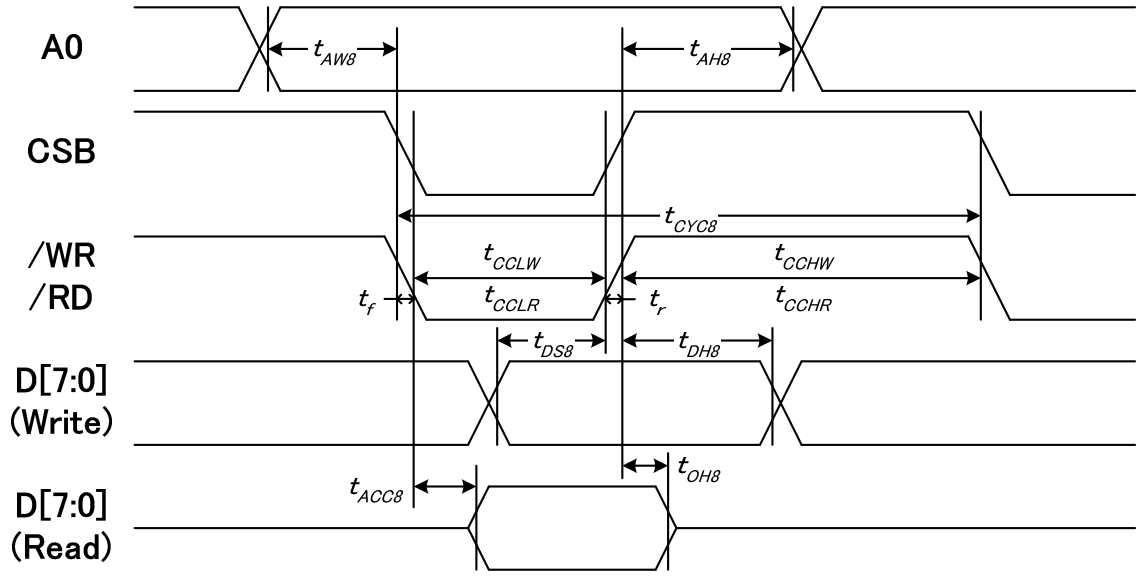
Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW6		0	—	ns
Address hold time		tAH6		0	—	
System cycle time	E	tCYC6		640	—	
Enable L pulse width (WRITE)		tEWLW		360	—	
Enable H pulse width (WRITE)		tEWHW		280	—	
Enable L pulse width (READ)		tEWLR		360	—	
Enable H pulse width (READ)		tEWHR		280	—	
Write data setup time	D[7:0]	tDS6		80	—	
Write data hold time		tDH6		20	—	
Read data access time		tACC6	CL = 16 pF	—	240	
Read data output disable time		tOH6	CL = 16 pF	10	200	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≦ (tCYC6 – tEWLW – tEWHW) for (tr + tf) ≦ (tCYC6 – tEWLR – tEWHR) are specified.

*2 All timing is specified using 20% and 80% of VDD1 as the reference.

*3 tEWLW and tEWLR are specified as the overlap between CSB being “L” and E.

14-2 System Bus Timing for 8080 Series MPU



(VDD1 = 3.3V , Ta =25˚C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW8		0	—	ns
Address hold time		tAH8		10	—	
System cycle time	/WR	tCYC8		240	—	
/WR L pulse width (WRITE)		tCCLW		80	—	
/WR H pulse width (WRITE)		tCCHW		80	—	
/RD L pulse width (READ)	RD	tCCLR		140	—	
/RD H pulse width (READ)		tCCHR		80	—	
WRITE Data setup time	D[7:0]	tDS8		40	—	
WRITE Data hold time		tDH8		20	—	
READ access time		tACC8	CL = 16 pF	—	70	
READ Output disable time		tOH8	CL = 16 pF	5	50	

(VDD1 = 2.8V , Ta =25˚C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW8		0	—	ns
Address hold time		tAH8		0	—	
System cycle time	/WR	tCYC8		400	—	
/WR L pulse width (WRITE)		tCCLW		220	—	
/WR H pulse width (WRITE)		tCCHW		180	—	
/RD L pulse width (READ)	RD	tCCLR		220	—	
/RD H pulse width (READ)		tCCHR		180	—	
WRITE Data setup time	D[7:0]	tDS8		40	—	
WRITE Data hold time		tDH8		20	—	
READ access time		tACC8	CL = 16 pF	—	140	
READ Output disable time		tOH8	CL = 16 pF	10	100	

(VDD1 = 1.8V , Ta =25˚C)

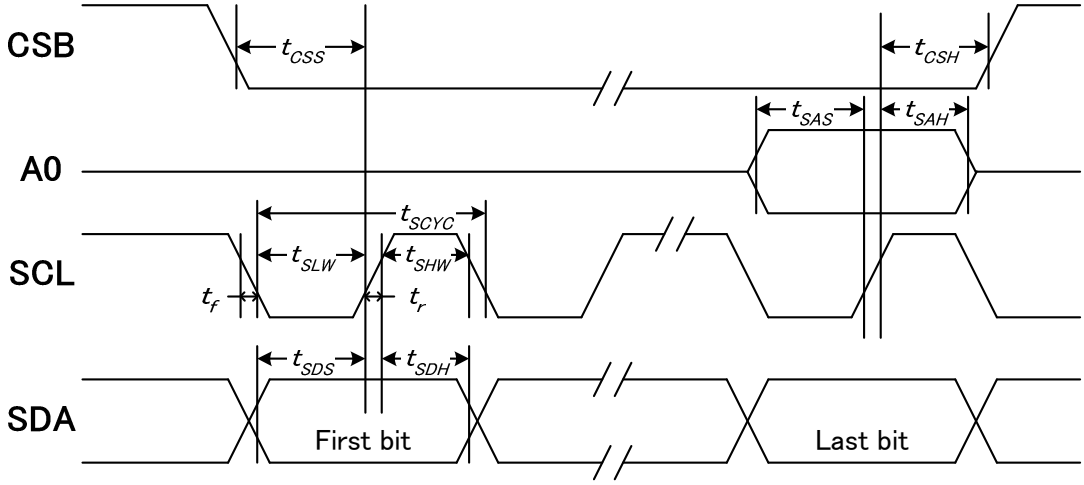
Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW8		0	—	ns
Address hold time		tAH8		0	—	
System cycle time	/WR	tCYC8		640	—	
/WR L pulse width (WRITE)		tCCLW		360	—	
/WR H pulse width (WRITE)		tCCHW		280	—	
/RD L pulse width (READ)	RD	tCCLR		360	—	
/RD H pulse width (READ)		tCCHR		280		
WRITE Data setup time	D[7:0]	tDS8		80	—	
WRITE Data hold time		tDH8		20	—	
READ access time		tACC8	CL = 16 pF	—	240	
READ Output disable time		tOH8	CL = 16 pF	10	200	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≦ (tCYC8 – tCCLW – tCCHW) for (tr + tf) ≦ (tCYC8 – tCCLR – tCCHR) are specified.

*2 All timing is specified using 20% and 80% of VDD1 as the reference.

*3 tCCLW and tCCLR are specified as the overlap between CSB being “L” and WR and RD being at the “L” level.

14-3 System Bus Timing for 4-Line Serial Interface



(VDD1 = 3.3V , Ta =25˚C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCL	tSCYC		50	—	ns
SCL “H” pulse width		tSHW		25	—	
SCL “L” pulse width		tSLW		25	—	
Address setup time	A0	tSAS		20	—	
Address hold time		tSAH		10	—	
Data setup time	SDA	tSDS		20	—	
Data hold time		tSDH		10	—	
CSB-SCL time	CSB	tCSS		20	—	
CSB-SCL time		tCSH		40	—	

(VDD1 = 2.8V , Ta =25˚C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCL	tSCYC		100	—	ns
SCL “H” pulse width		tSHW		50	—	
SCL “L” pulse width		tSLW		50	—	
Address setup time	A0	tSAS		30	—	
Address hold time		tSAH		20.	—	
Data setup time	SDA	tSDS		30	—	
Data hold time		tSDH		20	—	
CSB-SCL time	CSB	tCSS		30	—	
CSB-SCL time		tCSH		60	—	

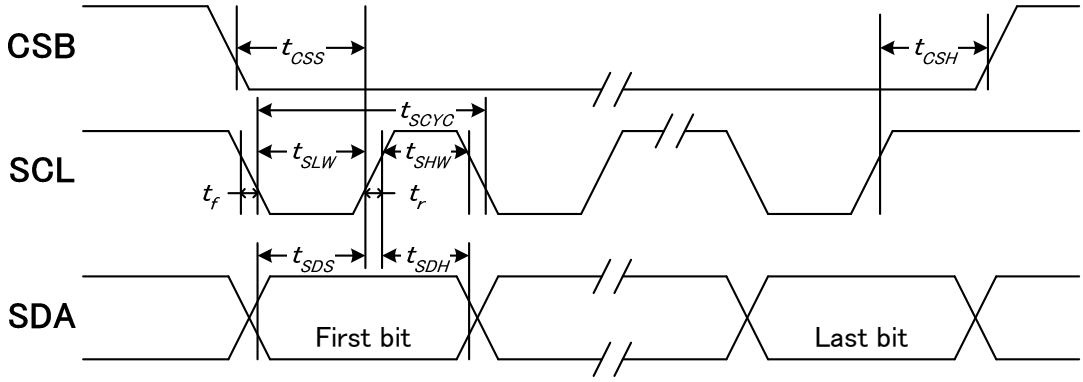
(VDD1 = 1.8V , Ta =25˚C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCL	tSCYC		200	—	ns
SCL “H” pulse width		tSHW		80	—	
SCL “L” pulse width		tSLW		80	—	
Address setup time	A0	tSAS		60	—	
Address hold time		tSAH		30	—	
Data setup time	SDA	tSDS		60	—	
Data hold time		tSDH		30	—	
CSB-SCL time	CSB	tCSS		40	—	
CSB-SCL time		tCSH		100	—	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of VDD1 as the standard.

14-4 SERIAL INTERFACE (3Line-SPI Interface)



(VDD1 = 3.3V , Ta =25˚C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCL	tSCYC		50	—	ns
SCL “H” pulse width		tSHW		25	—	
SCL “L” pulse width		tSLW		25	—	
Data setup time	SDA	tSDS		20	—	
Data hold time		tSDH		10	—	
CSB-SCL time	CSB	tCSS		20	—	
CSB-SCL time		tCSH		40	—	

(VDD1=2.8V Ta=25℃)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCL	tSCYC		100	—	ns
SCL “H” pulse width		tSHW		50	—	
SCL “L” pulse width		tSLW		50	—	
Data setup time	SDA	tSDS		30	—	
Data hold time		tSDH		20	—	
Chip select setup time	CSB	tCSS		30	—	
Chip select hold time		tCSH		60	—	

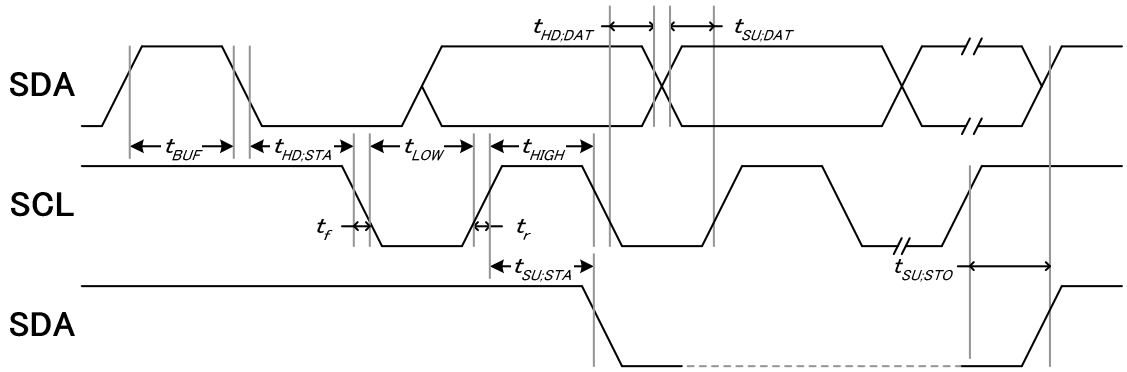
(VDD1 = 1.8V , Ta =25˚C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCL	tSCYC		200	—	ns
SCL “H” pulse width		tSHW		80	—	
SCL “L” pulse width		tSLW		80	—	
Data setup time	SDA	tSDS		60	—	
Data hold time		tSDH		30	—	
CSB-SCL time	CSB	tCSS		40	—	
CSB-SCL time		tCSH		100	—	

*1 The rise and fall time (tr, tf) of the input signal are specified at 15 ns or less.

*2 All timings take 20% and 80% of VDD1 as standard.

14-5 SERIAL INTERFACE (I2C Interface)



(VDD1 = 2.8V , Ta =25˚C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
SCL clock frequency	SCL	fSCL		-	400	kHZ
SCL clock low period		tLOW		160	-	ns
SCL clock high period		tHIGH		60	-	
Data set-up time	SDA	tSU;Data		80	-	
Data hold time		tHD;Data		40	-	
Setup time for a repeated START condition	SDA	tSU;STA		90	-	
Start condition hold time		tHD;STA		220	-	
Setup time for STOP condition		tSU;STO		110	-	
Bus free time between a STOP and START		tBUF		150	-	

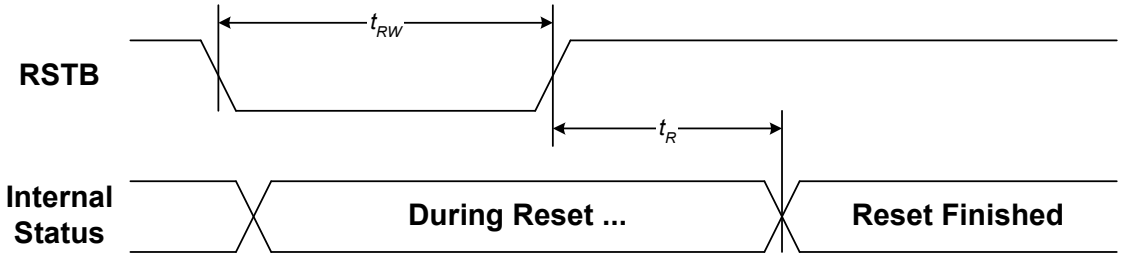
(VDD1 = 3.3V , Ta =25˚C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
SCL clock frequency	SCL	fSCL		-	400	kHZ
SCL clock low period		tLOW		160	-	ns
SCL clock high period		tHIGH		60	-	
Data set-up time	SDA	tSU;Data		80	-	
Data hold time		tHD;Data		40	-	
Setup time for a repeated START condition	SDA	tSU;STA		90	-	
Start condition hold time		tHD;STA		220	-	
Setup time for STOP condition		tSU;STO		110	-	
Bus free time between a STOP and START		tBUF		150	-	

*1 The rise and fall time (tr, tf) of the input signal are specified at 15 ns or less.

*2 All timings take 20% and 80% of VDD1 as standard.

14-6 Hardware Reset Timing



(VDD1 = 3.3V , Ta =25˚C)

Item	Symbol	Condition	Min.	Max.	Unit
Reset time	tR		—	1.0	us
Reset “L” pulse width	tRW		1.0	—	

(VDD1 = 2.8V , Ta =25˚C)

Item	Symbol	Condition	Min.	Max.	Unit
Reset time	tR		—	2.0	us
Reset “L” pulse width	tRW		2.0	—	

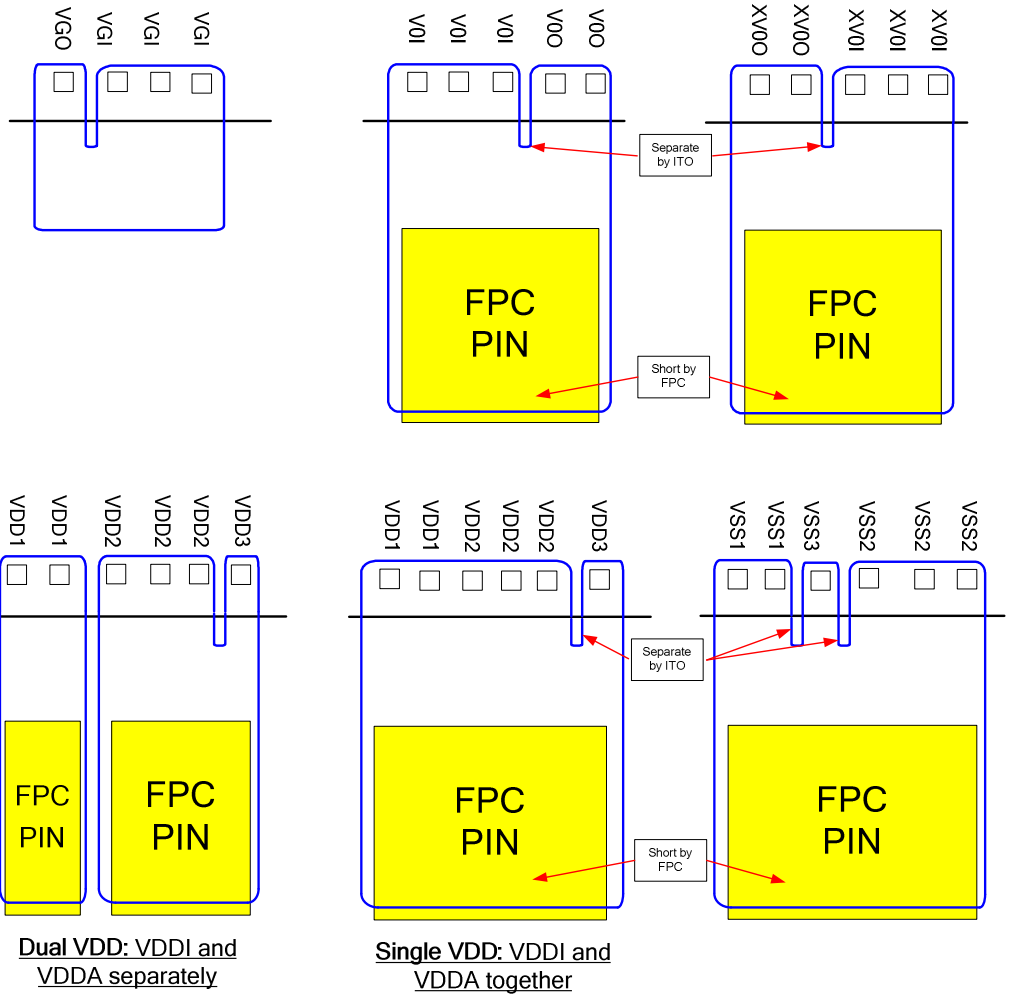
(VDD1 = 1.8V , Ta =25˚C)

Item	Symbol	Condition	Min.	Max.	Unit
Reset time	tR		—	3.0	us
Reset “L” pulse width	tRW		3.0	—	

15 APPLICATION NOTE

15-1 ITO Layout Reference

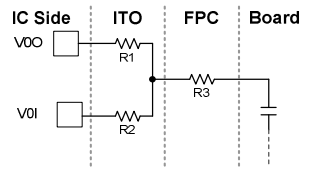
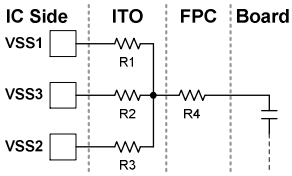
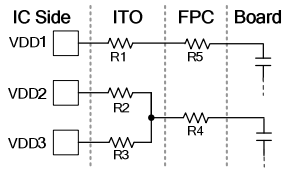
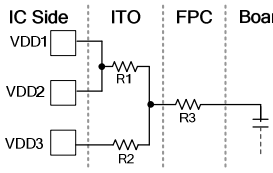
The reference ITO layout is shown below:



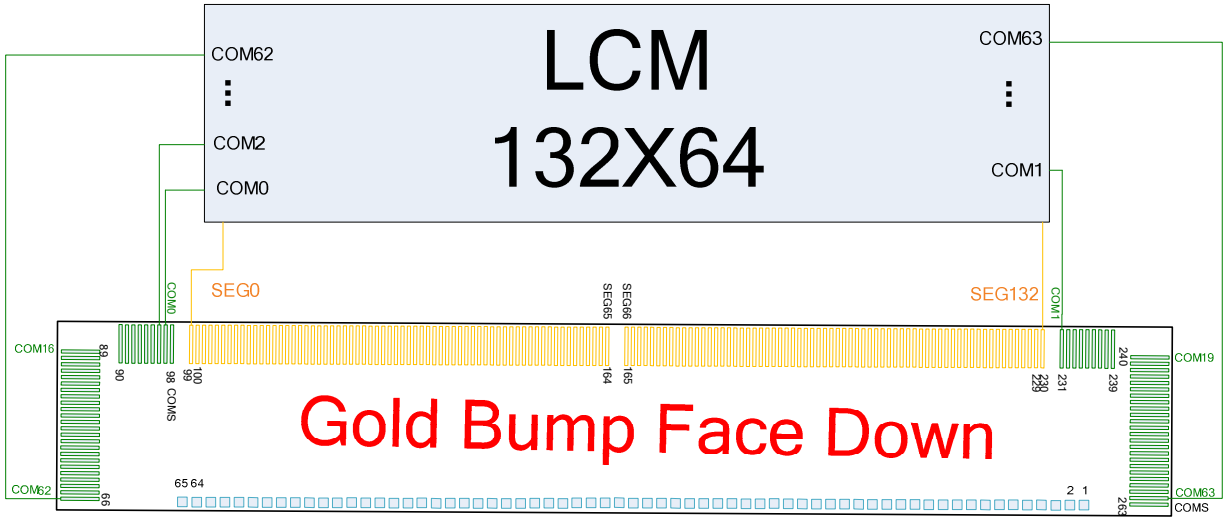
Dual VDD: VDDI and VDDA separately

Single VDD: VDDI and VDDA together

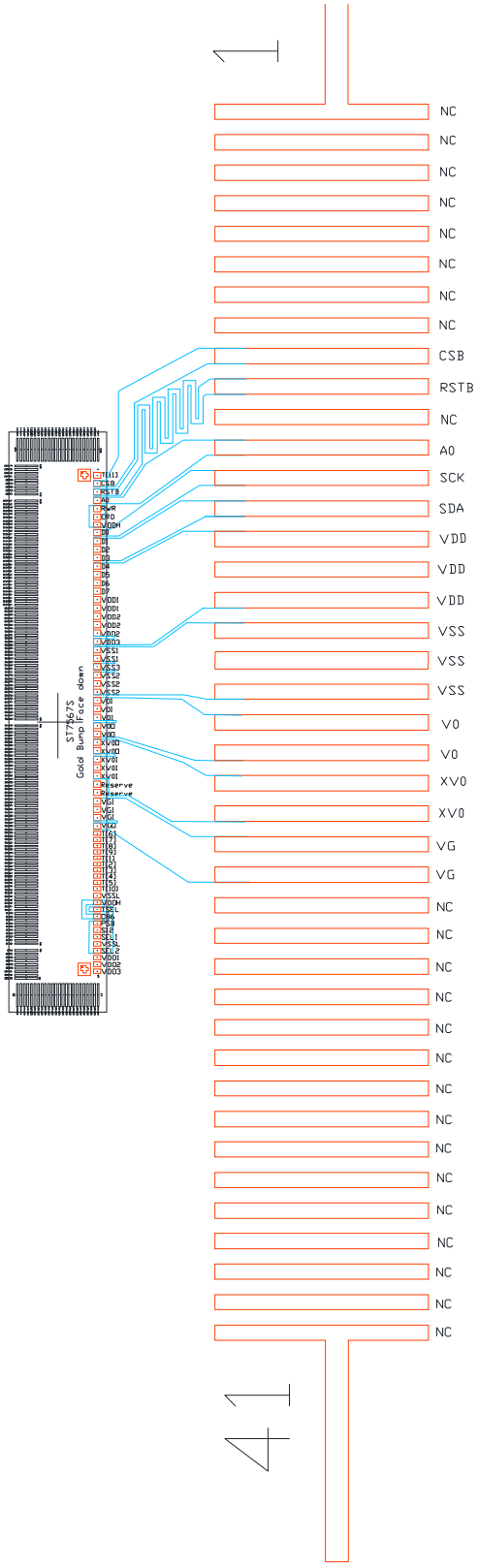
The equivalent circuit is shown below:

V0, XV0 & VG	*VSS*	*Dual VDD (VDDI & VDDA separately)*	*Single VDD (VDDI & VDDA together)*
			
Ideal Layout: => R3=0 Ohm. R1≥R2. **Acceptable Layout:** => R3≠0. R1>R2>R3. **Not Acceptable:** => R3 ≥ (R1 or R2). XV0 and VG are the same as V0.	**Ideal Layout:** => R4=0 Ohm. R2>>R1>R3. **Acceptable Layout:** => R4≠0. R2>>R1>R3>R4. **Not Acceptable:** => R4 ≥ (R1 or R2).	**Ideal Layout:** ⇨ R4=0 & R5=0 Ohm. ⇨ R3≧R1>R2. **Acceptable Layout:** ⇨ R4≠0 & R5≠0. ⇨ R3≧R1>R2>R5>R4 **Not Acceptable:** => R4 & R5 ≥ (R1 or R2 or R3).	**Ideal Layout:** => R3=0 Ohm. R2≥R1. **Acceptable Layout:** => R3≠0. R2≥R1>R3. **Not Acceptable:** => R3 ≥ (R1 or R2).

15-2 LCM Design Reference

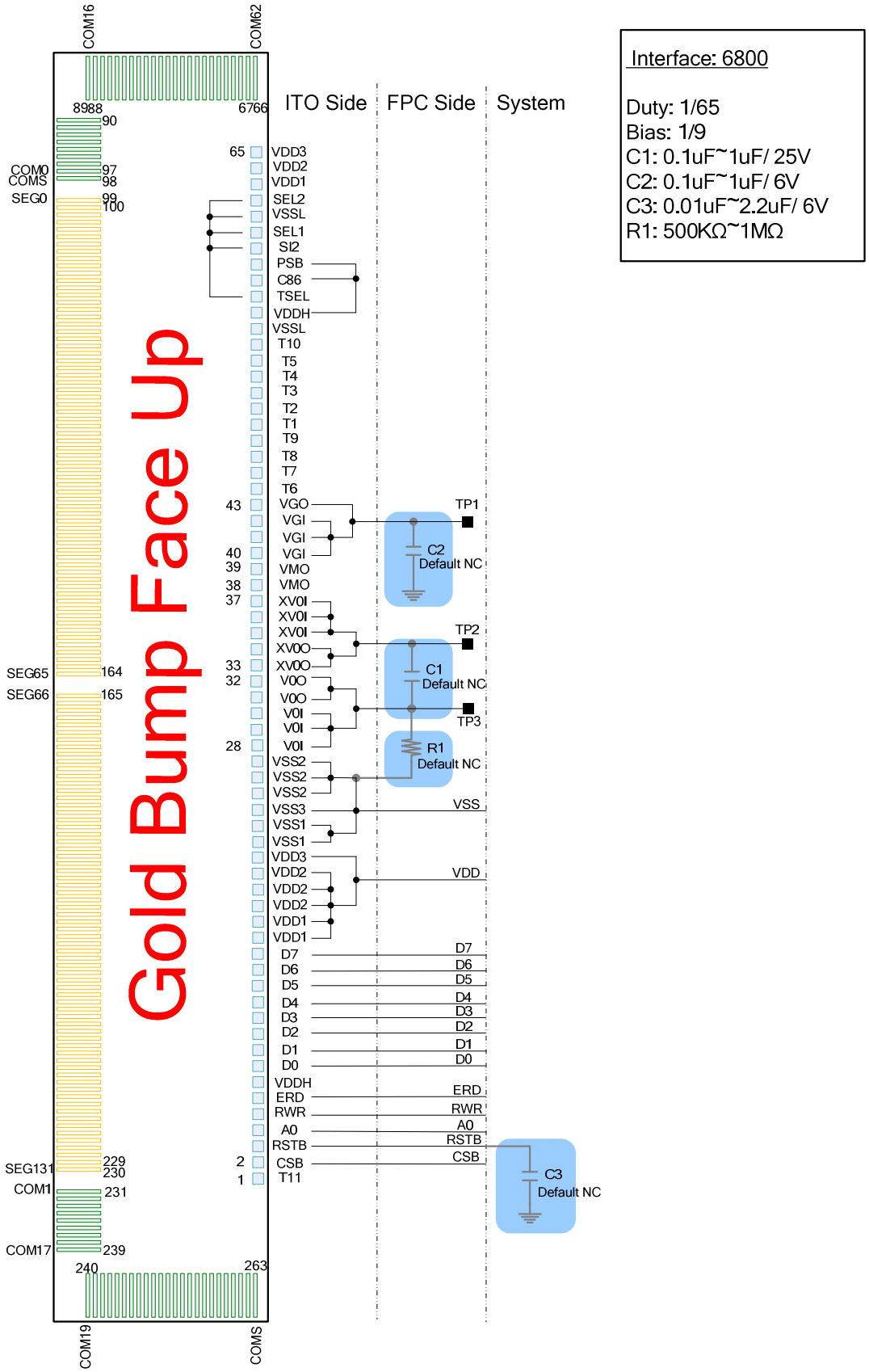


15-3 Layout Design Reference (65 Duty, 4line-SPI)



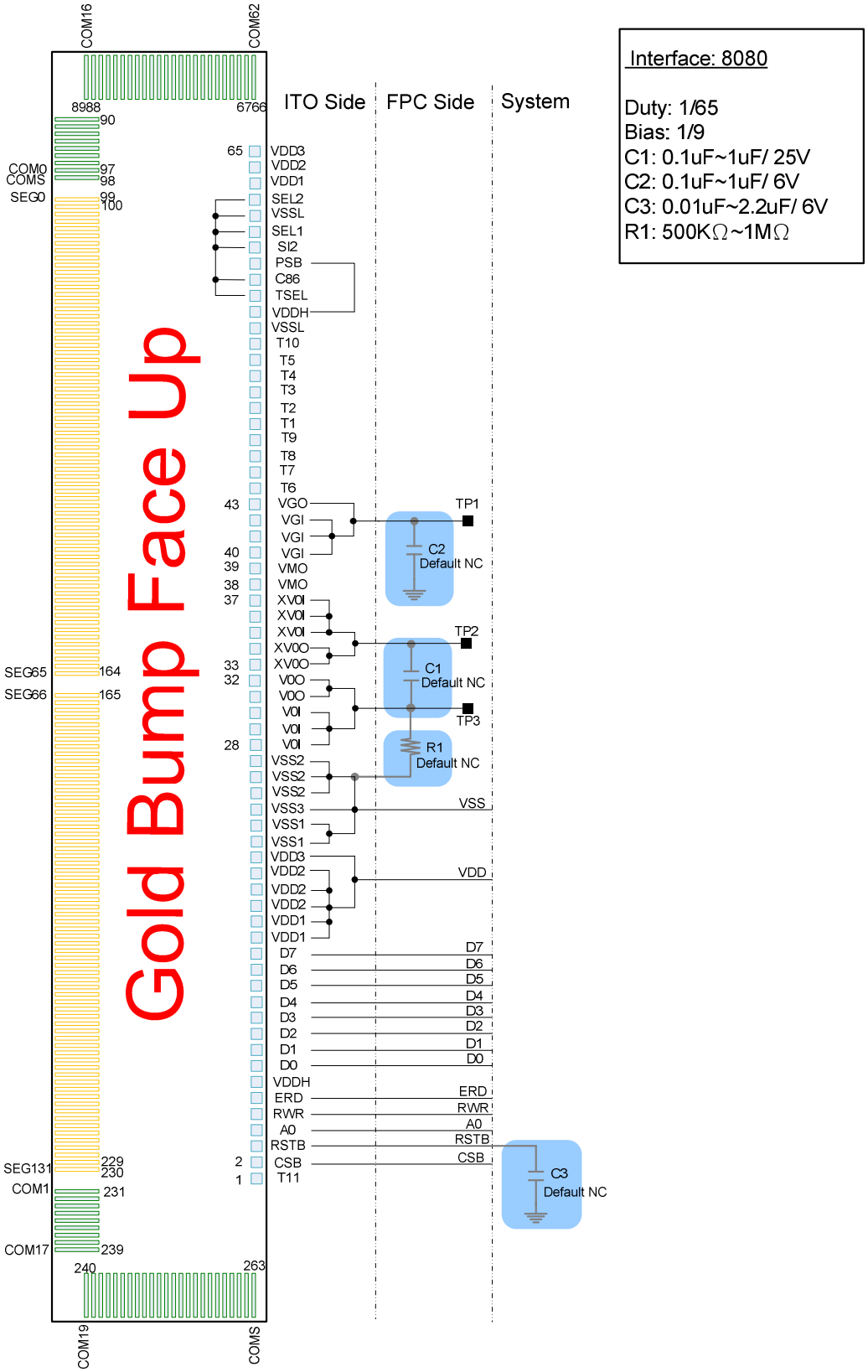
15-4 Application Circuit (6800 Interface)

If the panel size is larger than 2" or use the icon, must be added the capacitor C1 and C2, please refer to Section 7-8 External Components of Power Circuit.



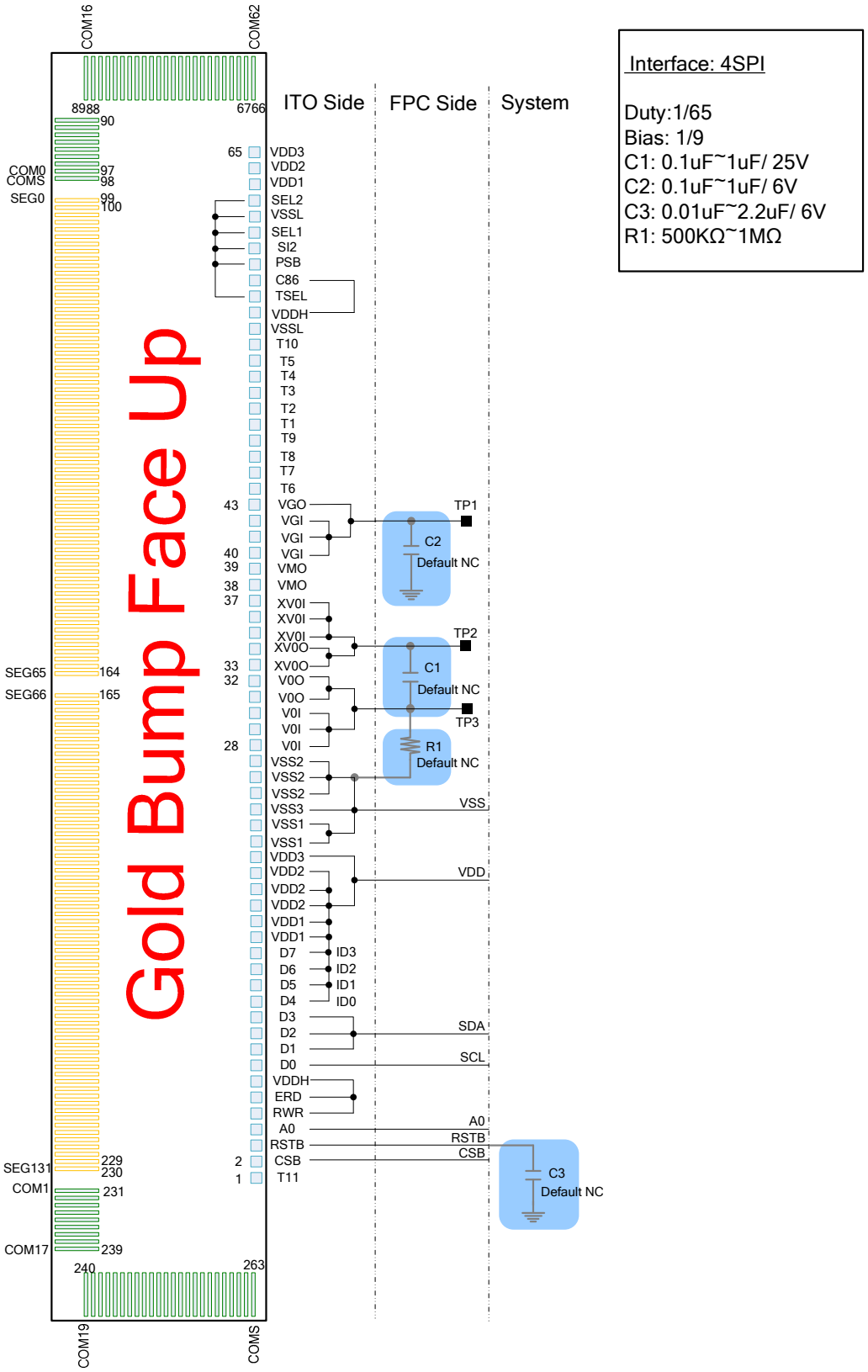
15-5 Application Circuit (8080 Interface)

If the panel size is larger than 2” or use the icon, must be added the capacitor C1 and C2, please refer to Section 7-8 External Components of Power Circuit.



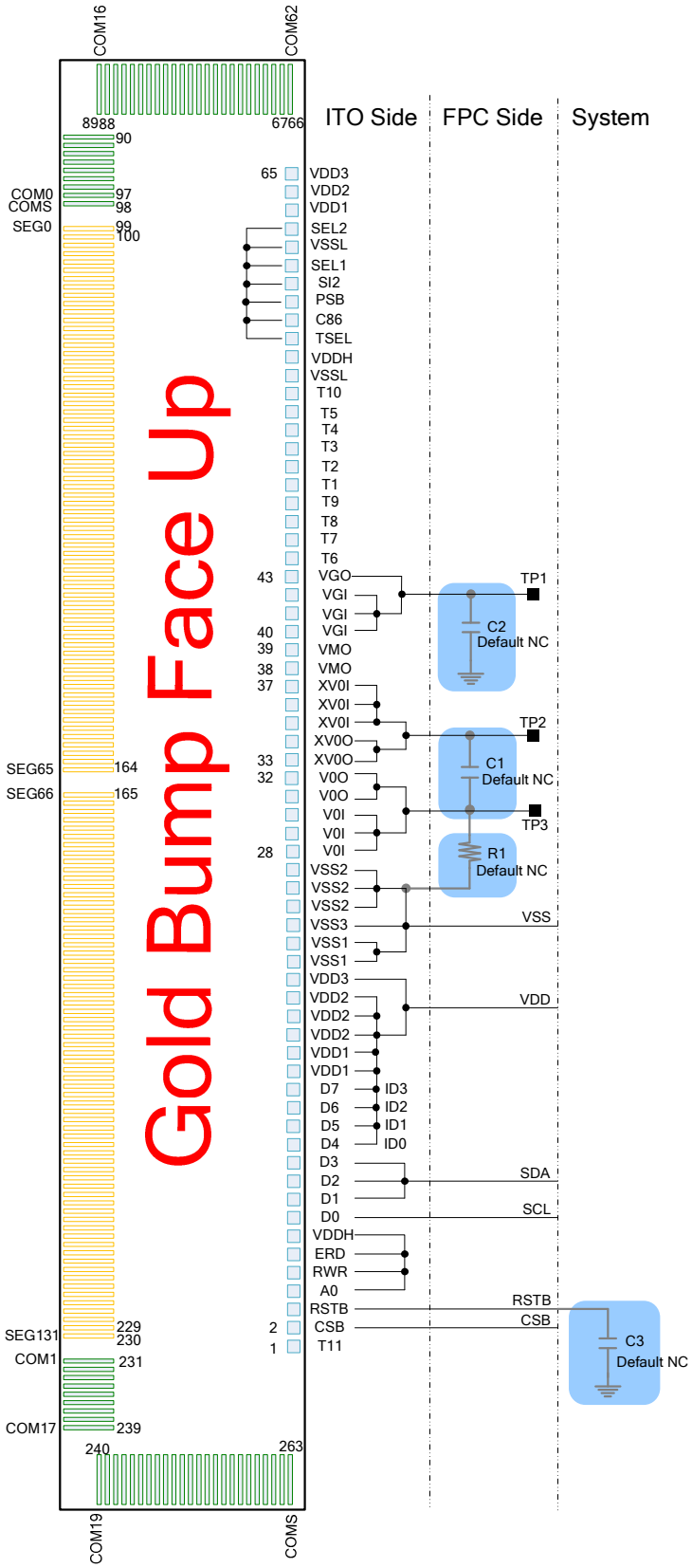
15-6 Application Circuit (4Line-SPI Interface)

If the panel size is larger than 2” or use the icon, must be added the capacitor C1 and C2, please refer to Section 7-8 External Components of Power Circuit.



15-7 Application Circuit (3Line-SPI Interface)

If the panel size is larger than 2” or use the icon, must be added the capacitor C1 and C2, please refer to Section 7-8 External Components of Power Circuit.

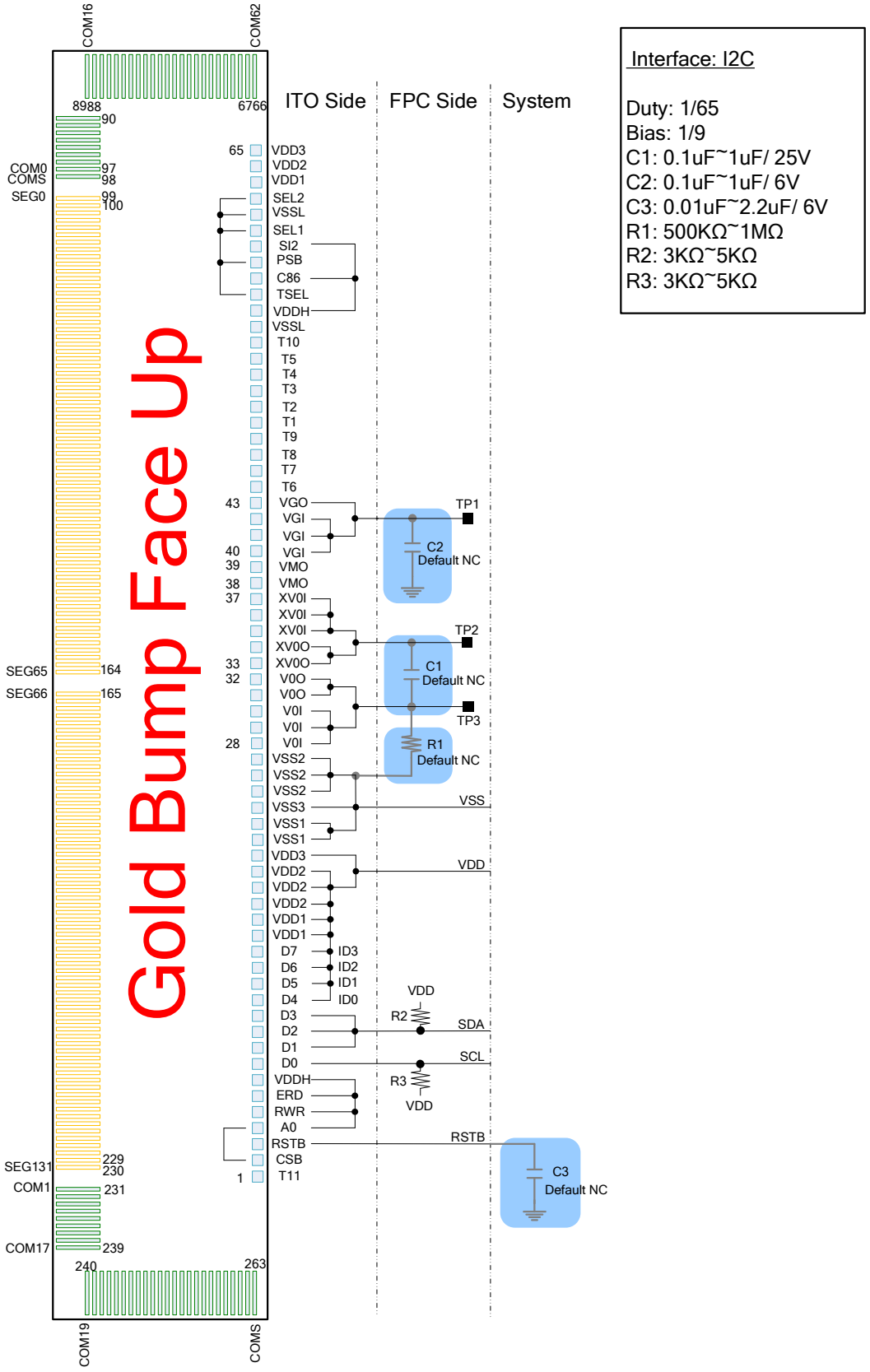


Interface: 3SPI

Duty: 1/65
Bias: 1/9
C1: 0.1uF~1uF/ 25V
C2: 0.1uF~1uF/ 6V
C3: 0.01uF~2.2uF/ 6V
R1: 500KΩ~1MΩ

15-8 Application Circuit (I2C-Interface)

If the panel size is larger than 2” or use the icon, must be added the capacitor C1 and C2, please refer to Section 7-8 External Components of Power Circuit.



16 REVERSION HISTORY

Version	Date	Description
1.0	2013/10/29	Formal Version.
1.0a	2014/02/18	Modify the Error Figure and DC Characteristic.
1.0b	2014/06/19	Modify DC Characteristic and Limiting Value.
1.0c	2014/06/25	Modify VLCD formula.
1.1	2014/07/08	Modify Error Command and Gold Bump Size.
1.1a	2014/07/09	Modify Power Circuit and Typing Error.
1.1b	2014/07/24	Modify Description Error.
1.2	2014/10/07	Modify Reference C Code of Power ON Flow and Refresh.
1.2a	2014/10/17	Modify Power Down Current (up to 4uA).
1.3	2014/10/29	1. Modify Part Number. 2. Modify Bump Height to 12um. 3. Modify Coordinates Typing Error. 4. Add Reset Reserve Capacitor and V0 Reserve Resistor. 5. Modify Reset Description in Power On Flow.
1.4	2016/07/13	Modify Column Address Instructions